EFM32PG22 Gecko MCU Family Data Sheet

The EFM32PG22 Gecko family of microcontrollers is part of the Series 2 Gecko portfolio. EFM32PG22 Gecko MCUs are ideal for enabling energy-friendly embedded applications.

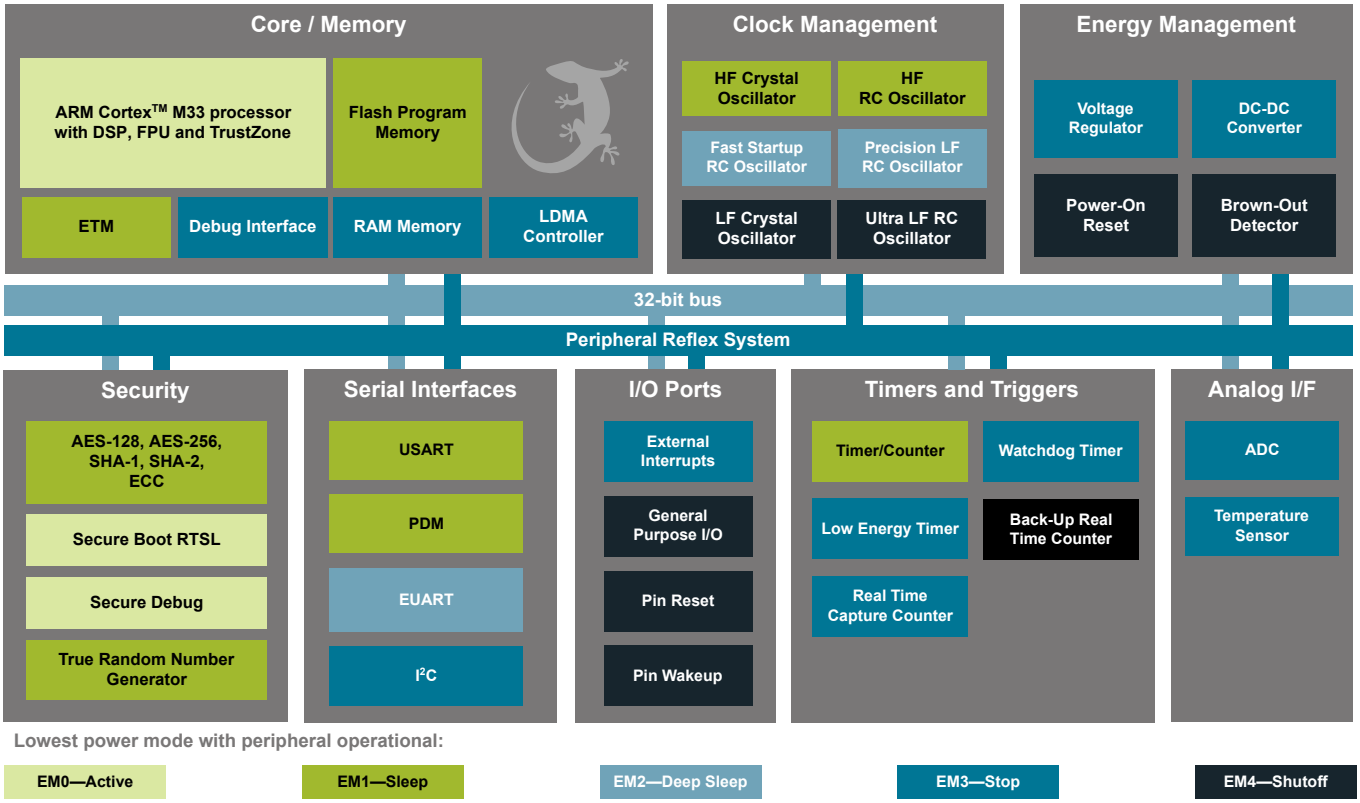
The highly efficient solution contains a 76.8 MHz Cortex-M33 with rich analog and communication peripherals to provide an industry-leading, energy efficient MCU for consumer and industrial applications.

Gecko applications include:

- Personal Hygiene devices
- Appliances and whitegoods
- Industrial Automation
- Consumer electronics

KEY FEATURES

- 32-bit ARM® Cortex®-M33 core with 76.8 MHz maximum operating frequency
- Up to 512 kB of flash and 32 kB of RAM
- Low energy operation
  - 26 uA/MHz (EM0)
  - 1.10 uA sleep (EM2)
- Secure Boot with Root of Trust and Secure Loader (RTSL)
- 16-bit ADC with 16-channel scan



1. Feature List

The EFM32PG22 highlighted features are listed below.

- **Low Power MCU**
  - High Performance 32-bit 76.8 MHz ARM Cortex®-M33 with DSP instruction and floating-point unit for efficient signal processing
  - Up to 512 kB flash program memory
  - Up to 32 kB RAM data memory
- **Low System Energy Consumption**
  - 26 µA/MHz in Active Mode (EM0) at 38.4 MHz
  - 1.10 µA EM2 DeepSleep current (8 kB RAM retention and RTC running from LFRCO)
  - 0.95 µA EM3 DeepSleep current (8 kB RAM retention and RTC running from ULFRCO)
  - 0.17 µA EM4 current
- **Security Features**
  - Secure Boot with Root of Trust and Secure Loader (RTSL)
  - Hardware Cryptographic Acceleration for AES128/256, SHA-1, SHA-2 (up to 256-bit), ECC (up to 256-bit), ECDSA, and ECDH
  - True Random Number Generator (TRNG) compliant with NIST SP800-90 and AIS-31
  - ARM® TrustZone®
  - Secure Debug with lock/unlock
- **Packages**
  - **QFN40** 5 mm × 5 mm × 0.85 mm
  - **QFN32** 4 mm × 4 mm × 0.85 mm
- **Wide selection of MCU peripherals**
  - Analog to Digital Converter (ADC)
    - 12-bit @ 1 Msps
    - 16-bit @ 76.9 ksps
  - Up to 26 General Purpose I/O pins with output state retention and asynchronous interrupts
  - 8 Channel DMA Controller
  - 12 Channel Peripheral Reflex System (PRS)
  - 4 × 16-bit Timer/Counter with 3 Compare/Capture/PWM channels
  - 1 × 32-bit Timer/Counter with 3 Compare/Capture/PWM channels
  - 32-bit Real Time Counter
  - 24-bit Low Energy Timer for waveform generation
  - 1 × Watchdog Timer
  - 2 × Universal Synchronous/Asynchronous Receiver/Transmitter (UART/SPI/SmartCard (ISO 7816)/IrDA/I^2S)
  - 1 × Enhanced Universal Asynchronous Receiver/Transmitter (EUART)
  - 2 × I^2C interface with SMBus support
  - Digital microphone interface (PDM)
  - Die temperature sensor with +/-1.5 °C accuracy after single-point calibration
- **Wide Operating Range**
  - 1.71 V to 3.8 V single power supply
  - -40 °C to 125 °C

2. Ordering Information

Table 2.1. Ordering Information

Ordering Code	Max CPU Speed	Flash (kB)	RAM (kB)	GPIO	Package	Temp Range
EFM32PG22C200F64IM40-C	76.8 MHz	64	32	26	QFN40	-40 to 125 °C
EFM32PG22C200F64IM32-C	76.8 MHz	64	32	18	QFN32	-40 to 125 °C
EFM32PG22C200F512IM40-C	76.8 MHz	512	32	26	QFN40	-40 to 125 °C
EFM32PG22C200F512IM32-C	76.8 MHz	512	32	18	QFN32	-40 to 125 °C
EFM32PG22C200F256IM40-C	76.8 MHz	256	32	26	QFN40	-40 to 125 °C
EFM32PG22C200F256IM32-C	76.8 MHz	256	32	18	QFN32	-40 to 125 °C
EFM32PG22C200F128IM40-C	76.8 MHz	128	32	26	QFN40	-40 to 125 °C
EFM32PG22C200F128IM32-C	76.8 MHz	128	32	18	QFN32	-40 to 125 °C

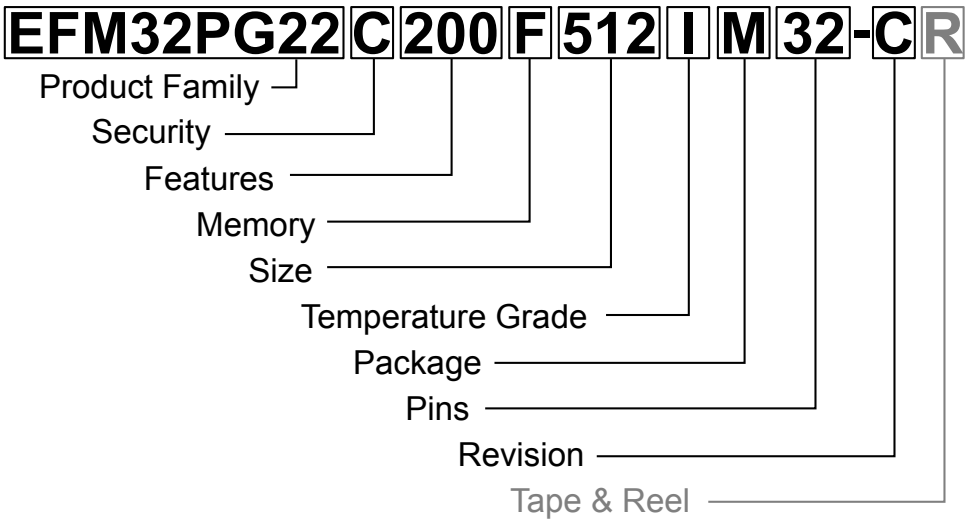


Figure 2.1. Ordering Code Key

Field	Options
Product Family	• **EFM32PG22**: Gecko 22 Family
Security	• **C**: Secure Boot with RTSL

Features [f1][f2][f3]	• f1
	  • **2**: MCU Frequency of 76.8 MHz
	• f2
	  • **0**: Unused
	• f3
	  • **0**: Unused

Memory	• **F**: Flash
Size	• **Memory Size** in kBytes
Temperature Grade	• **G**: -40 to +85 °C • **I**: -40 to +125 °C
Package	• **M**: QFN
Pins	• **Number of Package Pins**
Revision	• **C**: Revision C
Tape & Reel	• **R**: Tape & Reel (optional)

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3. System Overview

3.1 Introduction

The EFM32PG22 Gecko product family is well suited for any battery operated application as well as other systems requiring high performance and low energy consumption. This section gives a short introduction to the MCU system. The detailed functional description can be found in the EFM32PG22 Reference Manual.

A block diagram of the EFM32PG22 family is shown in Figure 3.1 Detailed EFM32PG22 Block Diagram on page 8. The diagram shows a superset of features available on the family, which vary by OPN. For more information about specific device features, consult 2. Ordering Information.

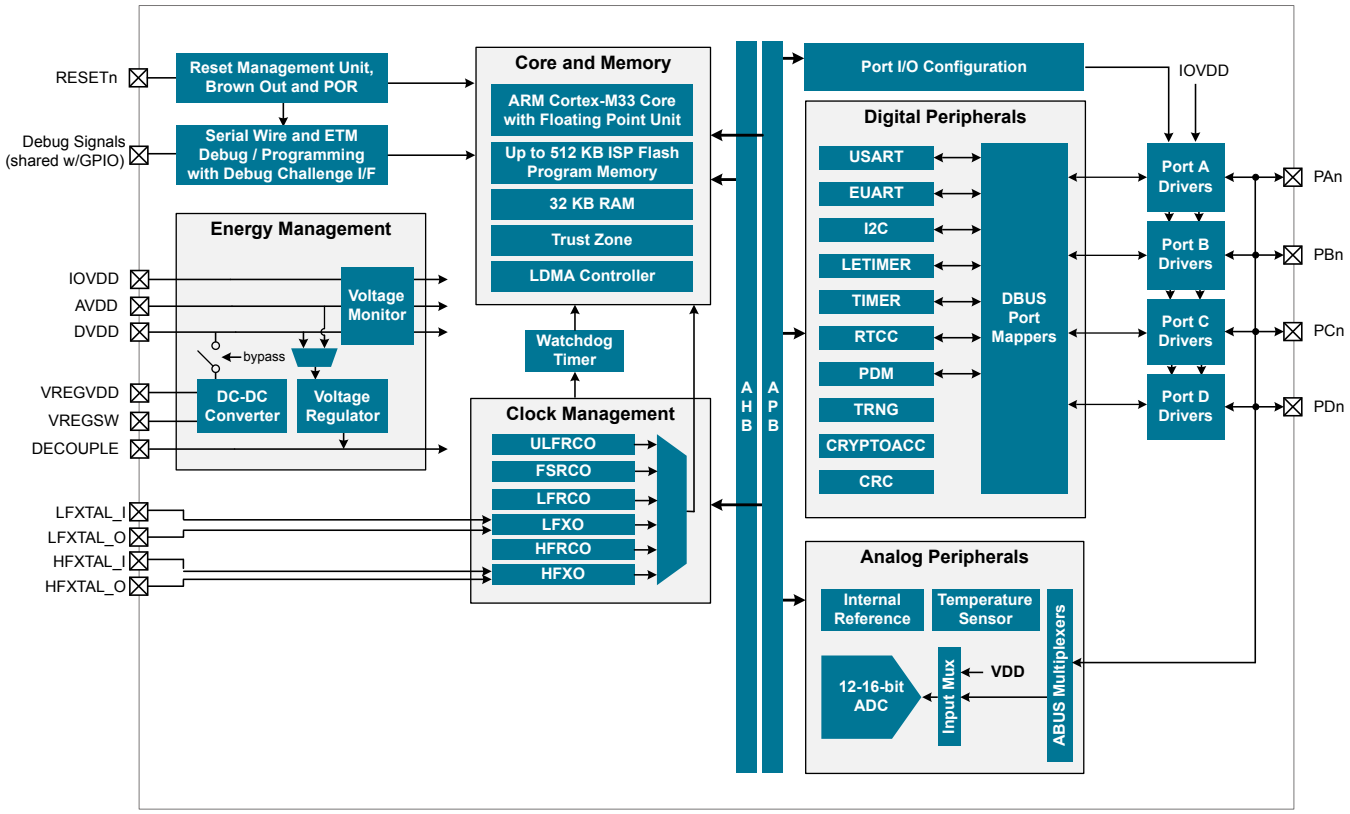

Figure 3.1. Detailed EFM32PG22 Block Diagram

3.2 General Purpose Input/Output (GPIO)

EFM32PG22 has up to 26 General Purpose Input/Output pins. Each GPIO pin can be individually configured as either an output or input. More advanced configurations including open-drain, open-source, and glitch-filtering can be configured for each individual GPIO pin. The GPIO pins can be overridden by peripheral connections, like SPI communication. Each peripheral connection can be routed to several GPIO pins on the device. The input value of a GPIO pin can be routed through the Peripheral Reflex System to other peripherals. The GPIO subsystem supports asynchronous external pin interrupts.

All of the pins on ports A and port B are EM2 capable. These pins may be used by Low-Energy peripherals in EM2/3 and may also be used as EM2/3 pin wake-ups. Pins on ports C and D are latched/retained in their current state when entering EM2 until EM2 exit upon which internal peripherals could once again drive those pads.

A few GPIOs also have EM4 wake functionality. These pins are listed in the Alternate Function Table.

3.3 Clocking

3.3.1 Clock Management Unit (CMU)

The Clock Management Unit controls oscillators and clocks in the EFM32PG22. Individual enabling and disabling of clocks to all peripheral modules is performed by the CMU. The CMU also controls enabling and configuration of the oscillators. A high degree of flexibility allows software to optimize energy consumption in any specific application by minimizing power dissipation in unused peripherals and oscillators.

3.3.2 Internal and External Oscillators

The EFM32PG22 supports two crystal oscillators and fully integrates four RC oscillators, listed below.

- A high frequency crystal oscillator (HFXO) with integrated load capacitors, tunable in small steps, provides a precise timing reference for the MCU. The HFXO can also support an external clock source such as a TCXO for applications that require an extremely accurate clock frequency over temperature.
- A 32.768 kHz crystal oscillator (LFXO) provides an accurate timing reference for low energy modes.
- An integrated high frequency RC oscillator (HFRCO) is available for the MCU system, when crystal accuracy is not required. The HFRCO employs fast start-up at minimal energy consumption combined with a wide frequency range, from 1 MHz to 76.8 MHz.
- An integrated fast start-up RC oscillator (FSRCO) that runs at a fixed 20 MHz
- An integrated low frequency 32.768 kHz RC oscillator (LFRCO) for low power operation without an external crystal. Precision mode enables periodic recalibration against the 38.4 MHz HFXO crystal to improve accuracy to +/- 500 ppm.
- An integrated ultra-low frequency 1 kHz RC oscillator (ULFRCO) is available to provide a timing reference at the lowest energy consumption in low energy modes.

3.4 Counters/Timers and PWM

3.4.1 Timer/Counter (TIMER)

TIMER peripherals keep track of timing, count events, generate PWM outputs and trigger timed actions in other peripherals through the Peripheral Reflex System (PRS). The core of each TIMER is a 16-bit or 32-bit counter with up to 3 compare/capture channels. Each channel is configurable in one of three modes. In capture mode, the counter state is stored in a buffer at a selected input event. In compare mode, the channel output reflects the comparison of the counter to a programmed threshold value. In PWM mode, the TIMER supports generation of pulse-width modulation (PWM) outputs of arbitrary waveforms defined by the sequence of values written to the compare registers. In addition some timers offer dead-time insertion.

See 3.12 Configuration Summary for information on the feature set of each timer.

3.4.2 Low Energy Timer (LETIMER)

The unique LETIMER is a 24-bit timer that is available in energy mode EM0 Active, EM1 Sleep, EM2 Deep Sleep, and EM3 Stop. This allows it to be used for timing and output generation when most of the device is powered down, allowing simple tasks to be performed while the power consumption of the system is kept at an absolute minimum. The LETIMER can be used to output a variety of waveforms with minimal software intervention. The LETIMER is connected to the Peripheral Reflex System (PRS), and can be configured to start counting on compare matches from other peripherals such as the Real Time Clock.

3.4.3 Real Time Clock with Capture (RTCC)

The Real Time Clock with Capture (RTCC) is a 32-bit counter providing timekeeping down to EM3. The RTCC can be clocked by any of the on-board low-frequency oscillators, and it is capable of providing system wake-up at user defined intervals.

3.4.4 Back-Up Real Time Counter (BURTC)

The Back-Up Real Time Counter (BURTC) is a 32-bit counter providing timekeeping in all energy modes, including EM4. The BURTC can be clocked by any of the on-board low-frequency oscillators, and it is capable of providing system wake-up at user-defined intervals.

3.4.5 Watchdog Timer (WDOG)

The watchdog timer can act both as an independent watchdog or as a watchdog synchronous with the CPU clock. It has windowed monitoring capabilities, and can generate a reset or different interrupts depending on the failure mode of the system. The watchdog can also monitor autonomous systems driven by the Peripheral Reflex System (PRS).

3.5 Communications and Other Digital Peripherals

3.5.1 Universal Synchronous/Asynchronous Receiver/Transmitter (USART)

The Universal Synchronous/Asynchronous Receiver/Transmitter is a flexible serial I/O module. It supports full duplex asynchronous UART communication with hardware flow control as well as RS-485, SPI, MicroWire and 3-wire. It can also interface with devices supporting:

- ISO7816 SmartCards
- IrDA
- I^2S

3.5.2 Enhanced Universal Asynchronous Receiver/Transmitter (EUART)

The Enhanced Universal Asynchronous Receiver/Transmitter supports full duplex asynchronous UART communication with hardware flow control, RS-485 and IrDA support. In EM0 and EM1 the EUART provides a high-speed, buffered communication interface.

When routed to GPIO ports A or B, the EUART may also be used in a low-energy mode and operate in EM2. A 32.768 kHz clock source allows full duplex UART communication up to 9600 baud.

3.5.3 Inter-Integrated Circuit Interface (I^2C)

The I^2C module provides an interface between the MCU and a serial I^2C bus. It is capable of acting as a main or secondary interface and supports multi-drop buses. Standard-mode, fast-mode and fast-mode plus speeds are supported, allowing transmission rates from 10 kbit/s up to 1 Mbit/s. Bus arbitration and timeouts are also available, allowing implementation of an SMBus-compliant system. The interface provided to software by the I^2C module allows precise timing control of the transmission process and highly automated transfers. Automatic recognition of addresses is provided in active and low energy modes. Note that not all instances of I^2C are available in all energy modes.

3.5.4 Peripheral Reflex System (PRS)

The Peripheral Reflex System provides a communication network between different peripheral modules without software involvement. Peripheral modules producing Reflex signals are called producers. The PRS routes Reflex signals from producers to consumer peripherals which in turn perform actions in response. Edge triggers and other functionality such as simple logic operations (AND, OR, NOT) can be applied by the PRS to the signals. The PRS allows peripherals to act autonomously without waking the MCU core, saving power.

3.5.5 Pulse Density Modulation (PDM) Interface

The PDM module provides a serial interface and decimation filter for Pulse Density Modulation (PDM) microphones, isolated Sigma-delta ADCs, digital sensors and other PDM or sigma delta bit stream peripherals. A programmable Cascaded Integrator Comb (CIC) filter is used to decimate the incoming bit streams. PDM supports stereo or mono input data and DMA transfer.

3.6 Security Features

The EFM32PG22 supports the following extended Secure Vault Mid features:

Table 3.1. Secure Vault Features

Feature	Secure Vault Mid
True Random Number Generator (TRNG)	Yes
Secure Boot with Root of Trust and Secure Loader (RTSL)	Yes
Secure Debug with Lock/Unlock	Yes
DPA Countermeasures	No
Secure Attestation	Using TrustZone
Secure Key Management	Using TrustZone
Symmetric Encryption	• AES 128 / 192 / 256 bit • ECB, CTR, CBC, CFB, CCM, GCM, CBC-MAC, and GMAC
Public Key Encryption - ECDSA / ECDH /	• p192 and p256
Key Derivation	• ECJ-PAKE p192 and p256
Hashes	• SHA-1 • SHA2/224 • SHA-2/256

3.6.1 Secure Boot with Root of Trust and Secure Loader (RTSL)

The Secure Boot with RTSL authenticates a chain of trusted firmware that begins from an immutable memory (ROM).

It prevents malware injection, prevents rollback, ensures that only authentic firmware is executed.

More information on this feature can be found in the Application Note *AN1218: Series 2 Secure Boot with RTSL*.

3.6.2 Cryptographic Accelerator

The Cryptographic Accelerator is an autonomous hardware accelerator which supports AES encryption and decryption with 128/192/256-bit keys, Elliptic Curve Cryptography (ECC) to support public key operations and hashes.

Supported block cipher modes of operation for AES include:

- ECB (Electronic Code Book)
- CTR (Counter Mode)
- CBC (Cipher Block Chaining)
- CFB (Cipher Feedback)
- GCM (Galois Counter Mode)
- CBC-MAC (Cipher Block Chaining Message Authentication Code)
- GMAC (Galois Message Authentication Code)
- CCM (Counter with CBC-MAC)

The Cryptographic Accelerator accelerates Elliptical Curve Cryptography and supports the NIST (National Institute of Standards and Technology) recommended curves including P-192 and P-256 for ECDH(Elliptic Curve Diffie-Hellman) key derivation and ECDSA (Elliptic Curve Digital Signature Algorithm) sign and verify operations.

Supported hashes include SHA-1, SHA2/224, and SHA-2/256.

This implementation provides a fast and energy efficient solution to state of the art cryptographic needs.

3.6.3 True Random Number Generator

The True Random Number Generator module is a non-deterministic random number generator that harvests entropy from a thermal energy source. It includes start-up health tests for the entropy source as required by NIST SP800-90B and AIS-31 as well as online health tests required for NIST SP800-90C.

The TRNG is suitable for periodically generating entropy to seed an approved pseudo random number generator.

3.6.4 Secure Debug with Lock/Unlock

For obvious security reasons, it is critical for a product to have its debug interface locked before being released in the field.

In addition, the EFM32PG22 also provides a secure debug unlock function that allows authenticated access based on public key cryptography. This functionality is particularly useful for supporting failure analysis while maintaining confidentiality of IP and sensitive end-user data.

More information on this feature can be found in AN1190: Series 2 Secure Debug.

3.7 Analog

3.7.1 Analog to Digital Converter (IADC)

The IADC is a hybrid architecture combining techniques from both SAR and Delta-Sigma style converters. It has a resolution of 12 bits at 1 Msps and 16 bits at up to 76.9 ksps. Hardware oversampling reduces system-level noise over multiple front-end samples. The IADC includes integrated voltage reference options. Inputs are selectable from a wide range of sources, including pins configurable as either single-ended or differential.

3.8 Power

The EFM32PG22 has an Energy Management Unit (EMU) and efficient integrated regulators to generate internal supply voltages. Only a single external supply voltage is required, from which all internal voltages are created. An optional integrated DC-DC buck regulator can be utilized to further reduce the current consumption. The DC-DC regulator requires one external inductor and one external capacitor.

The EFM32PG22 device family includes support for internal supply voltage scaling, as well as two different power domains groups for peripherals. These enhancements allow for further supply current reductions and lower overall power consumption.

3.8.1 Energy Management Unit (EMU)

The Energy Management Unit manages transitions of energy modes in the device. Each energy mode defines which peripherals and features are available and the amount of current the device consumes. The EMU can also be used to implement system-wide voltage scaling and turn off the power to unused RAM blocks to optimize the energy consumption in the target application. The DC-DC regulator operation is tightly integrated with the EMU.

3.8.2 Voltage Scaling

The EFM32PG22 supports supply voltage scaling for the LDO powering DECOUPLE, with independent selections for EM0 / EM1 and EM2 / EM3. Voltage scaling helps to optimize the energy efficiency of the system by operating at lower voltages when possible. The EM0 / EM1 voltage scaling level defaults to VSCALE2, which allows the core to operate in active mode at full speed. The intermediate level, VSCALE1, allows operation in EM0 and EM1 at up to 40 MHz. The lowest level, VSCALE0, can be used to conserve power further in EM2 and EM3. The EMU will automatically switch the target voltage scaling level when transitioning between energy modes.

3.8.3 DC-DC Converter

The DC-DC buck converter covers a wide range of load currents, provides high efficiency in energy modes EM0, EM1, EM2 and EM3, and can supply up to 60 mA for device operation. An on-chip supply-monitor signals when the supply voltage is low to allow bypass of the regulator via programmable software interrupt. It employs soft switching at boot and DCDC regulating-to-bypass transitions to limit the max supply slew-rate and mitigate inrush current.

3.8.4 Power Domains

The EFM32PG22 has three peripheral power domains for operation in EM2 and EM3, as well as the ability to selectively retain configurations for EM0/EM1 peripherals. A small set of peripherals always remain powered on in EM2 and EM3, including all peripherals which are available in EM4. If all of the peripherals in PD0B or PD0C are configured as unused, that power domain will be powered off in EM2 or EM3, reducing the overall current consumption of the device. Likewise, if the application can tolerate the setup time to re-configure used EM0/EM1 peripherals on wake, register retention for these peripherals can be disabled to further reduce the EM2 or EM3 current.

Table 3.2. Peripheral Power Subdomains

Always available in EM2/EM3	Power Domain PD0B	Power Domain PD0C
RTCC	LETIMER0	LFRCO (Precision Mode)
LFRCO (Non-precision mode)[1]	IADC0	
LFXO[1]	I2C0	
BURTC[1]	WDOG0	
ULFRCO[1]	EUART0	
FSRCO	PRS	
	DEBUG	

Note:
1. Peripheral also available in EM4.

3.9 Reset Management Unit (RMU)

The RMU is responsible for handling reset of the EFM32PG22. A wide range of reset sources are available, including several power supply monitors, pin reset, software controlled reset, core lockup reset, and watchdog reset.

3.10 Core and Memory

3.10.1 Processor Core

The ARM Cortex-M processor includes a 32-bit RISC processor integrating the following features and tasks in the system:

- ARM Cortex-M33 RISC processor achieving 1.50 Dhrystone MIPS/MHz
- ARM TrustZone security technology
- Embedded Trace Macrocell (ETM) for real-time trace and debug
- Up to 512 KB flash program memory
- Up to 32 KB RAM data memory
- Configuration and event handling of all modules
- 2-pin Serial-Wire debug interface

3.10.2 Memory System Controller (MSC)

The Memory System Controller (MSC) is the program memory unit of the microcontroller. The flash memory is readable and writable from both the Cortex-M33 and LDMA. In addition to the main flash array where Program code is normally written the MSC also provides an Information block where additional information such as special user information or flash-lock bits are stored. There is also a read-only page in the information block containing system and device calibration data. Read and write operations are supported in energy modes EM0 Active and EM1 Sleep.

3.10.3 Linked Direct Memory Access Controller (LDMA)

The Linked Direct Memory Access (LDMA) controller allows the system to perform memory operations independently of software. This reduces both energy consumption and software workload. The LDMA allows operations to be linked together and staged, enabling sophisticated operations to be implemented.

3.11 Memory Map

The EFM32PG22 memory map is shown in the figures below. RAM and flash sizes are for the largest memory configuration.

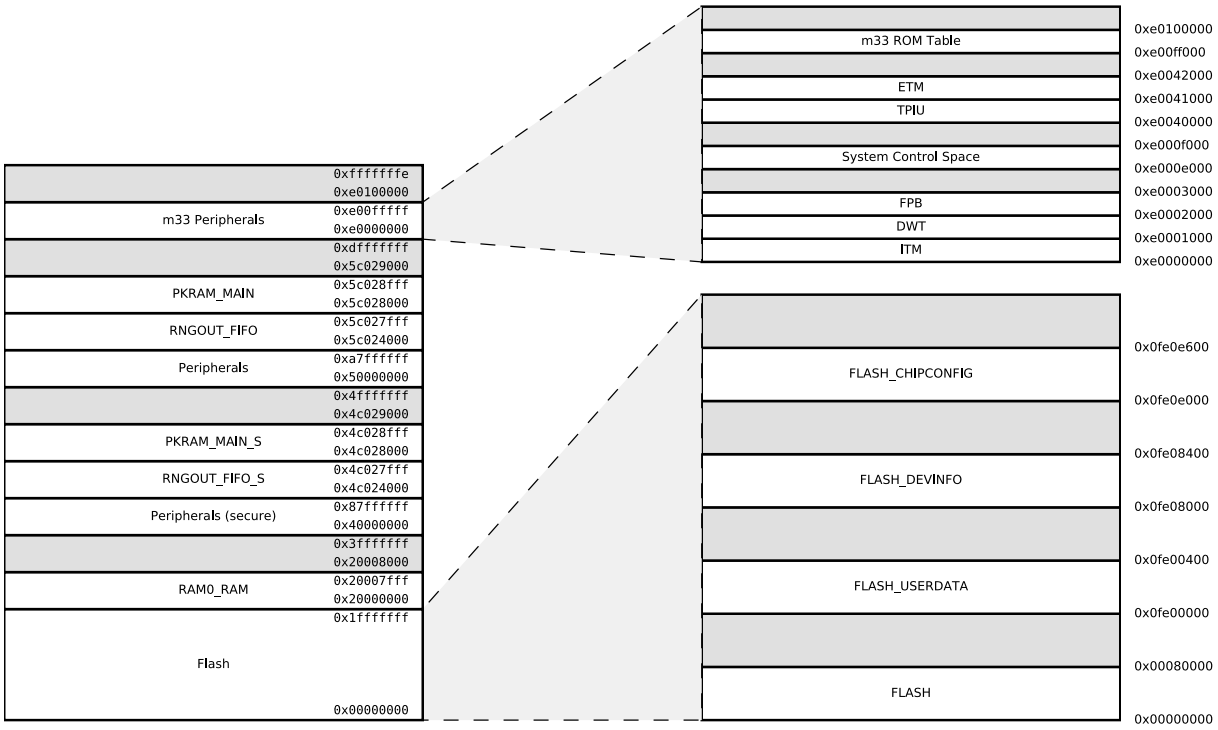

Figure 3.2. EFM32PG22 Memory Map — Core Peripherals and Code Space

3.12 Configuration Summary

The features of the EFM32PG22 are a subset of the feature set described in the device reference manual. The table below describes device specific implementation of the features. Remaining modules support full configuration.

Table 3.3. Configuration Summary

Module	Lowest Energy Mode	Configuration
I2C0	EM3[1]	
I2C1	EM1	
IADC0	EM3	
LETIMER0	EM2[1]	
PDM	EM1	2-channel
TIMER0	EM1	32-bit, 3-channels, +DTI
TIMER1	EM1	16-bit, 3-channels, +DTI
TIMER2	EM1	16-bit, 3-channels, +DTI
TIMER3	EM1	16-bit, 3-channels, +DTI
TIMER4	EM1	16-bit, 3-channels, +DTI
EUART0	EM1 - Full high-speed operation EM3[1] - Low-energy operation, 9600 Baud	
USART0	EM1	+IrDA, +I2S, +SmartCard
USART1	EM1	+IrDA, +I2S, +SmartCard

Note:

1. EM2 and EM3 operation is only supported for digital peripheral I/O on Port A and Port B. All GPIO ports support digital peripheral operation in EM0 and EM1.

4. Electrical Specifications

4.1 Electrical Characteristics

All electrical parameters in all tables are specified under the following conditions, unless stated otherwise:

- Typical values are based on T_A=25 °C and all supplies at 3.0 V, by production test and/or technology characterization.
- Minimum and maximum values represent the worst conditions across supply voltage, process variation, and operating temperature, unless stated otherwise.

Power Supply Pin Dependencies

Due to on-chip circuitry (e.g., diodes), some EFM32 power supply pins have a dependent relationship with one or more other power supply pins. These internal relationships between the external voltages applied to the various EFM32 supply pins are defined below. Exceeding the below constraints can result in damage to the device and/or increased current draw.

- VREGVDD & DVDD
  - In systems using the DCDC converter, DVDD (the buck converter output) should be connected to the recommended L_{DCDC} and C_{DCDC}, and should not be driven by an off-chip regulator.
  - In systems not using the DCDC converter, DVDD must be shorted to VREGVDD on the PCB (VREGVDD=DVDD)
- DVDD ≥ DECOUPLE
- AVDD, IOVDD: No dependency with each other or any other supply pin. Additional leakage may occur if DVDD remains unpowered with power applied to these supplies.

4.2 Absolute Maximum Ratings

Stresses beyond those listed below may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at those or any other conditions beyond those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. For more information on the available quality and reliability data, see the Quality and Reliability Monitor Report at http://www.silabs.com/support/quality/pages/default.aspx.

Table 4.1. Absolute Maximum Ratings

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Storage temperature range	T_{STG}		-50	—	+150	°C
Voltage on any supply pin[1]	V_{DDMAX}		-0.3	—	3.8	V
Junction temperature	T_{JMAX}	-I grade	—	—	+125	°C
Voltage ramp rate on any supply pin	$V_{DDRAMPMAX}$		—	—	1.0	V / µs
Voltage on HFXO pins	$V_{HFXOPIN}$		-0.3	—	1.2	V
DC voltage on any GPIO pin	V_{DIGPIN}		-0.3	—	V_{IOVDD} + 0.3	V
DC voltage on RESETn pin[2]	V_{RESETn}		-0.3	—	3.8	V
Total current into VDD power lines	I_{VDDMAX}	Source	—	—	200	mA
Total current into VSS ground lines	I_{VSSMAX}	Sink	—	—	200	mA
Current per I/O pin	I_{IOMAX}	Sink	—	—	50	mA
		Source	—	—	50	mA
Current for all I/O pins	$I_{IOALLMAX}$	Sink	—	—	200	mA
		Source	—	—	200	mA

Note:

1. The maximum supply voltage on VREGVDD is limited under certain conditions when using the DC-DC. See the DC-DC specifications for more details.
2. The RESETn pin has a pull-up device to the DVDD supply. For minimum leakage, RESETn should not exceed the voltage at DVDD.

4.3 General Operating Conditions

Table 4.2. General Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Operating ambient temperature range	T_A	-I temperature grade [1]	-40	—	+125	° C
DVDD supply voltage	V_{DVDD}	EM0/1	1.71	3.0	3.8	V
		EM2/3/4[2]	1.71	3.0	3.8	V
AVDD supply voltage	V_{AVDD}		1.71	3.0	3.8	V
IOVDDx operating supply voltage (All IOVDD pins)	V_{IOVDDx}		1.71	3.0	3.8	V
VREGVDD operating supply voltage	$V_{VREGVDD}$	DC-DC in regulation[3]	2.2	3.0	3.8	V
		DC-DC in bypass 60 mA load	1.8	3.0	3.8	V
		DC-DC not in use. DVDD externally shorted to VREGVDD	1.71	3.0	3.8	V
DECOUPLE output capacitor[4]	$C_{DECOUPLE}$	1.0 µF ± 10% X8L capacitor used for performance characterization.	1.0	—	2.75	µF
HCLK and SYSCLK frequency	f_{HCLK}	VSCALE2, MODE = WS1	—	—	76.8	MHz
		VSCALE2, MODE = WS0	—	—	40	MHz
PCLK frequency	f_{PCLK}	VSCALE2	—	—	50	MHz
		VSCALE1	—	—	40	MHz
EM01 Group A clock frequency	$f_{EM01GRPACLK}$	VSCALE2	—	—	76.8	MHz
		VSCALE1	—	—	40	MHz
EM01 Group B clock frequency	$f_{EM01GRPBCLK}$	VSCALE2	—	—	76.8	MHz
		VSCALE1	—	—	40	MHz
External Clock Input	f_{CLKIN}	VSCALE2 or VSCALE1	—	—	40	MHz
DPLL Reference Clock	$f_{DPLLREFCLK}$	VSCALE2 or VSCALE1	—	—	40	MHz

Note:

1. The device may operate continuously at the maximum allowable ambient T_A rating as long as the absolute maximum T_{JMAX} is not exceeded. For an application with significant power dissipation, the allowable T_A may be lower than the maximum T_A rating. T_A = T_{JMAX} - ($THETA_{JA}$ x PowerDissipation). Refer to the Absolute Maximum Ratings table and the Thermal Characteristics table for T_{JMAX} and $THETA_{JA}$.
2. The DVDD supply is monitored by the DVDD BOD in EM0/1 and the LE DVDD BOD in EM2/3/4.
3. The maximum supply voltage on VREGVDD is limited under certain conditions when using the DC-DC. See the DC-DC specifications for more details.
4. Murata GCM21BL81C105KA58L used for performance characterization. Actual capacitor values can be significantly de-rated from their specified nominal value by the rated tolerance, as well as the application's AC voltage, DC bias, and temperature. The minimum capacitance counting all error sources should be no less than 0.6 µF.

4.4 DC-DC Converter

Test conditions: L_{DCDC} = 2.2 µH (Samsung CIG22H2R2MNE), C_{DCDC} = 4.7 µF (Samsung CL10B475KQ8NQNC), $V_{VREGVDD}$ = 3.0 V, V_{OUT} = 1.8 V, IPKVAL in EM0/1 modes is set to 150 mA, and in EM2/3 modes is set to 90 mA, unless otherwise indicated.

Table 4.3. DC-DC Converter

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input voltage range at VREGVDD pin[1]	$V_{VREGVDD}$	DCDC in regulation, I_{LOAD} = 60 mA, EM0/EM1 mode	2.2	3.0	3.8*	V
		DCDC in regulation, I_{LOAD} = 5 mA, EM0/EM1 or EM2/EM3 mode	1.8	3.0	3.8*	V
		Bypass mode	1.8	3.0	3.8	V
Regulated output voltage	V_{OUT}		—	1.8	—	V
Regulation DC accuracy	ACC_{DC}	$V_{VREGVDD}$ ≥ 2.2 V, Steady state in EM0/EM1 mode or EM2/EM3 mode	-2.5	—	3.3	%
Regulation total accuracy	ACC_{TOT}	With mode transitions between EM0/EM1 and EM2/EM3 modes	-5	—	7	%
Steady-state output ripple	V_R	I_{LOAD} = 20 mA in EM0/EM1 mode	—	14.3	—	mVpp
DC line regulation	V_{REG}	I_{LOAD} = 60 mA in EM0/EM1 mode, $V_{VREGVDD}$ ≥ 2.2 V	—	5.5	—	mV/V
DC load regulation	I_{REG}	Load current between 100 µA and 60 mA in EM0/EM1 mode	—	0.27	—	mV/mA
Efficiency	EFF	Load current between 100 µA and 60 mA in EM0/EM1 mode, or between 10 µA and 5 mA in EM2/EM3 mode	—	91	—	%
Output load current	I_{LOAD}	EM0/EM1 mode, DCDC in regulation	—	—	60	mA
		EM2/EM3 mode, DCDC in regulation	—	—	5	mA
		Bypass mode	—	—	60	mA
Nominal output capacitor	C_{DCDC}	4.7 µF ± 10% X7R capacitor used for performance characterization[2]	4.7	—	10	µF
Nominal inductor	L_{DCDC}	± 20% tolerance	—	2.2	—	µH
Nominal input capacitor	C_{IN}		C_{DCDC}	—	—	µF
Resistance in bypass mode	R_{BYP}	Bypass switch from VREGVDD to DVDD, $V_{VREGVDD}$ = 1.8 V	—	1.75	3	Ω
		Powertrain PFET switch from VREGVDD to VREGSW, $V_{VREGVDD}$ = 1.8 V	—	0.86	1.5	Ω
Supply monitor threshold programming range	V_{CMP_RNG}	Programmable in 0.1 V steps	2.0	—	2.3	V
Supply monitor threshold accuracy	V_{CMP_ACC}	Supply falling edge trip point	-5	—	5	%

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply monitor threshold hysteresis	V_{CMP_HYST}	Positive hysteresis on the supply rising edge referred to the falling edge trip point	—	4	—	%
Supply monitor response time	t_{CMP_DELAY}	Supply falling edge at -100 mV / µs	—	0.6	—	µs

Note:

1. The supported maximum $V_{VREGVDD}$ in regulation mode is a function of temperature and 10-year lifetime average load current. See more details in 4.4.1 DC-DC Operating Limits.
2. Samsung CL10B475KQ8NQNC used for performance characterization. Actual capacitor values can be significantly de-rated from their specified nominal value by the rated tolerance, as well as the application's AC voltage, DC bias, and temperature. The minimum capacitance counting all error sources should be no less than 2.4 µF.

4.4.1 DC-DC Operating Limits

The maximum supported voltage on the VREGVDD supply pin is limited under certain conditions. Maximum input voltage is a function of temperature and the average load current over a 10-year lifetime. Figure 4.1 Lifetime average load current limit vs. Maximum input voltage on page 22 shows the safe operating region under specific conditions. Exceeding this safe operating range may impact the reliability and performance of the DC-DC converter.

The average load current for an application can typically be determined by examining the current profile during the time the device is powered. For example, an application that is continuously powered which spends 99% of the time asleep consuming 2 µA and 1% of the time active and consuming 10 mA has an average lifetime load current of about 102 µA.

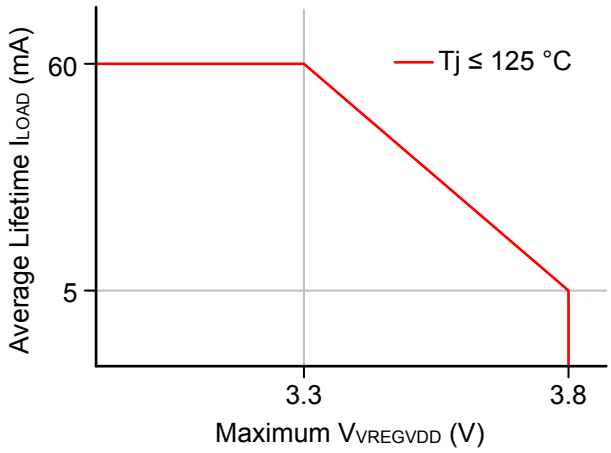

Figure 4.1. Lifetime average load current limit vs. Maximum input voltage

The minimum input voltage for the DC-DC in EM0/EM1 mode is a function of the maximum load current, and the peak current setting. Figure 4.2 Transient maximum load current vs. Minimum input voltage on page 22 shows the max load current vs. input voltage for different DC-DC peak inductor current settings.

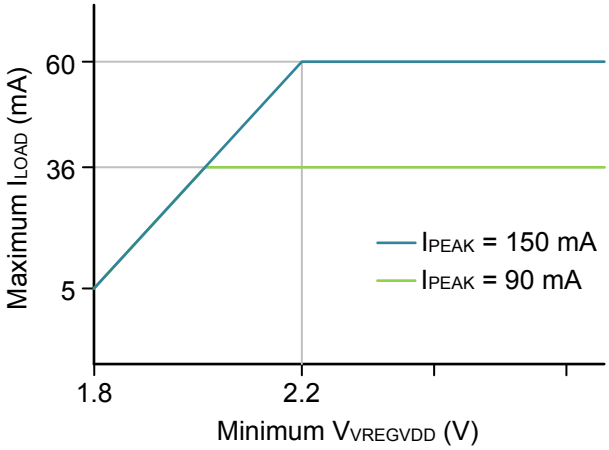

Figure 4.2. Transient maximum load current vs. Minimum input voltage

4.5 Thermal Characteristics

Table 4.4. Thermal Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Thermal Resistance Junction to Ambient QFN32 (4x4mm) Package	$THE-TA_{JA\_QFN32\_4X4}$	4-Layer PCB, Natural Convection[1]	—	35.4	—	°C/W
Thermal Resistance, Junction to Ambient, QFN40 (5x5mm) Package	$THE-TA_{JA\_QFN40\_5X5}$	4-Layer PCB, Natural Convection[1]	—	32.6	—	°C/W

Note:

1. Measured according to JEDEC standard JESD51-2A. Integrated Circuit Thermal Test Method Environmental Conditions - Natural Convection (Still Air).

4.6 Current Consumption

4.6.1 MCU current consumption using DC-DC at 3.0 V input

Unless otherwise indicated, typical conditions are: VREGVDD = 3.0 V. AVDD = DVDD = IOVDD = 1.8 V from DC-DC. Voltage scaling level = VSCALE1. T_A = 25 °C. Minimum and maximum values in this table represent the worst conditions across process variation at T_A = 25 °C.

Table 4.5. MCU current consumption using DC-DC at 3.0 V input

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM0 mode with all peripherals disabled	I_{ACTIVE}	76.8 MHz HFRCO w/ DPLL referenced to 38.4 MHz crystal, CPU running Prime from flash, VSCALE2	—	28	—	µA/MHz
		76.8 MHz HFRCO w/ DPLL referenced to 38.4 MHz crystal, CPU running while loop from flash, VSCALE2	—	27	—	µA/MHz
		76.8 MHz HFRCO w/ DPLL referenced to 38.4 MHz crystal, CPU running CoreMark loop from flash, VSCALE2	—	37	—	µA/MHz
		38.4 MHz crystal, CPU running Prime from flash	—	28	—	µA/MHz
		38.4 MHz crystal, CPU running while loop from flash	—	26	—	µA/MHz
		38.4 MHz crystal, CPU running CoreMark loop from flash	—	38	—	µA/MHz
		38 MHz HFRCO, CPU running while loop from flash	—	22	—	µA/MHz
		26 MHz HFRCO, CPU running while loop from flash	—	24	—	µA/MHz
		16 MHz HFRCO, CPU running while loop from flash	—	27	—	µA/MHz
		1 MHz HFRCO, CPU running while loop from flash	—	159	—	µA/MHz
Current consumption in EM1 mode with all peripherals disabled	I_{EM1}	76.8 MHz HFRCO w/ DPLL referenced to 38.4 MHz crystal, VSCALE2	—	17	—	µA/MHz
		38.4 MHz crystal	—	17	—	µA/MHz
		38 MHz HFRCO	—	13	—	µA/MHz
		26 MHz HFRCO	—	15	—	µA/MHz
		16 MHz HFRCO	—	18	—	µA/MHz
		1 MHz HFRCO	—	150	—	µA/MHz

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM2 mode, VSCALE0	I_{EM2_VS}	Full RAM retention and RTC running from LFXO	—	1.30	—	µA
		Full RAM retention and RTC running from LFRCO	—	1.30	—	µA
		Full RAM retention and RTC running from LFRCO in precision mode	—	1.65	—	µA
		24 kB RAM retention and RTC running from LFXO	—	1.22	—	µA
		24 kB RAM retention and RTC running from LFRCO in precision mode	—	1.56	—	µA
		8 kB RAM retention and RTC running from LFXO	—	1.11	—	µA
		8 kB RAM retention and RTC running from LFRCO	—	1.10	—	µA
		8 kB RAM retention and RTC running from LFXO, CPU cache not retained	—	1.03	—	µA
Current consumption in EM3 mode, VSCALE0	I_{EM3_VS}	8 kB RAM retention and RTC running from ULFRCO	—	0.95	—	µA
Additional current in EM2 or EM3 when any peripheral in PD0B is enabled[1]	I_{PD0B_VS}		—	0.37	—	µA

Note:

1. Extra current consumed by power domain. Does not include current associated with the enabled peripherals. See 3.8.4 Power Domains for a list of the peripherals in each power domain.

4.6.2 MCU current consumption at 3.0 V

Unless otherwise indicated, typical conditions are: AVDD = DVDD = IOVDD = VREGVDD = 3.0 V. DC-DC not used. Voltage scaling level = VSCALE1. T_A = 25 °C. Minimum and maximum values in this table represent the worst conditions across process variation at T_A = 25 °C.

Table 4.6. MCU current consumption at 3.0 V

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM0 mode with all peripherals disabled	I_{ACTIVE}	76.8 MHz HFRCO w/ DPLL referenced to 38.4 MHz crystal, CPU running Prime from flash, VSCALE2	—	42	—	µA/MHz
		76.8 MHz HFRCO w/ DPLL referenced to 38.4 MHz crystal, CPU running while loop from flash, VSCALE2	—	39	—	µA/MHz
		76.8 MHz HFRCO w/ DPLL referenced to 38.4 MHz crystal, CPU running CoreMark loop from flash, VSCALE2	—	54	—	µA/MHz
		38.4 MHz crystal, CPU running Prime from flash	—	40	—	µA/MHz
		38.4 MHz crystal, CPU running while loop from flash	—	39	—	µA/MHz
		38.4 MHz crystal, CPU running CoreMark loop from flash	—	55	—	µA/MHz
		38 MHz HFRCO, CPU running while loop from flash	—	33	50	µA/MHz
		26 MHz HFRCO, CPU running while loop from flash	—	35	—	µA/MHz
		16 MHz HFRCO, CPU running while loop from flash	—	40	—	µA/MHz
		1 MHz HFRCO, CPU running while loop from flash	—	228	830	µA/MHz
Current consumption in EM1 mode with all peripherals disabled	I_{EM1}	76.8 MHz HFRCO w/ DPLL referenced to 38.4 MHz crystal, VSCALE2	—	24	—	µA/MHz
		38.4 MHz crystal	—	25	—	µA/MHz
		38 MHz HFRCO	—	19	35	µA/MHz
		26 MHz HFRCO	—	21	—	µA/MHz
		16 MHz HFRCO	—	27	—	µA/MHz
		1 MHz HFRCO	—	215	770	µA/MHz

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM2 mode, VSCALE0	I_{EM2_VS}	Full RAM retention and RTC running from LFXO	—	1.74	—	µA
		Full RAM retention and RTC running from LFRCO	—	1.75	4.9	µA
		24 kB RAM retention and RTC running from LFXO	—	1.61	—	µA
		24 kB RAM retention and RTC running from LFRCO in precision mode	—	2.14	—	µA
		8 kB RAM retention and RTC running from LFXO	—	1.44	—	µA
		8 kB RAM retention and RTC running from LFRCO	—	1.45	—	µA
		8 kB RAM retention and RTC running from LFXO, CPU cache not retained	—	1.39	—	µA
Current consumption in EM3 mode, VSCALE0	I_{EM3_VS}	8 kB RAM retention and RTC running from ULFRCO	—	1.21	3.7	µA
Current consumption in EM4 mode	I_{EM4}	No BURTC, no LF oscillator	—	0.17	0.43	µA
		BURTC with LFXO	—	0.50	—	µA
Current consumption during reset	I_{RST}	Hard pin reset held	—	234	—	µA
Additional current in EM2 or EM3 when any peripheral in PD0B is enabled[1]	I_{PD0B_VS}		—	0.56	—	µA

Note:

1. Extra current consumed by power domain. Does not include current associated with the enabled peripherals. See 3.8.4 Power Domains for a list of the peripherals in each power domain.

4.6.3 MCU current consumption at 1.8 V

Unless otherwise indicated, typical conditions are: AVDD = DVDD = IOVDD = VREGVDD = 1.8 V. DC-DC not used. Voltage scaling level = VSCALE1. T_A = 25 °C. Minimum and maximum values in this table represent the worst conditions across process variation at T_A = 25 °C.

Table 4.7. MCU current consumption at 1.8 V

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM0 mode with all peripherals disabled	I_{ACTIVE}	76.8 MHz HFRCO w/ DPLL referenced to 38.4 MHz crystal, CPU running Prime from flash, VSCALE2	—	42	—	µA/MHz
		76.8 MHz HFRCO w/ DPLL referenced to 38.4 MHz crystal, CPU running while loop from flash, VSCALE2	—	39	—	µA/MHz
		76.8 MHz HFRCO w/ DPLL referenced to 38.4 MHz crystal, CPU running CoreMark loop from flash, VSCALE2	—	54	—	µA/MHz
		38.4 MHz crystal, CPU running Prime from flash	—	41	—	µA/MHz
		38.4 MHz crystal, CPU running while loop from flash	—	39	—	µA/MHz
		38.4 MHz crystal, CPU running CoreMark loop from flash	—	55	—	µA/MHz
		38 MHz HFRCO, CPU running while loop from flash	—	33	—	µA/MHz
		26 MHz HFRCO, CPU running while loop from flash	—	35	—	µA/MHz
		16 MHz HFRCO, CPU running while loop from flash	—	40	—	µA/MHz
		1 MHz HFRCO, CPU running while loop from flash	—	227	—	µA/MHz
Current consumption in EM1 mode with all peripherals disabled	I_{EM1}	76.8 MHz HFRCO w/ DPLL referenced to 38.4 MHz crystal, VSCALE2	—	24	—	µA/MHz
		38.4 MHz crystal	—	25	—	µA/MHz
		38 MHz HFRCO	—	19	—	µA/MHz
		26 MHz HFRCO	—	21	—	µA/MHz
		16 MHz HFRCO	—	27	—	µA/MHz
		1 MHz HFRCO	—	213	—	µA/MHz

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM2 mode, VSCALE0	I_{EM2_VS}	Full RAM retention and RTC running from LFXO	—	1.67	—	µA
		Full RAM retention and RTC running from LFRCO	—	1.66	—	µA
		24 kB RAM retention and RTC running from LFXO	—	1.53	—	µA
		24 kB RAM retention and RTC running from LFRCO in precision mode	—	2.06	—	µA
		8 kB RAM retention and RTC running from LFXO	—	1.37	—	µA
		8 kB RAM retention and RTC running from LFRCO	—	1.36	—	µA
		8 kB RAM retention and RTC running from LFXO, CPU cache not retained	—	1.32	—	µA
Current consumption in EM3 mode, VSCALE0	I_{EM3_VS}	8 kB RAM retention and RTC running from ULFRCO	—	1.14	—	µA
Current consumption in EM4 mode	I_{EM4}	No BURTC, no LF oscillator	—	0.13	—	µA
		BURTC with LFXO	—	0.44	—	µA
Current consumption during reset	I_{RST}	Hard pin reset held	—	190	—	µA
Additional current in EM2 or EM3 when any peripheral in PD0B is enabled[1]	I_{PD0B_VS}		—	0.54	—	µA

Note:

1. Extra current consumed by power domain. Does not include current associated with the enabled peripherals. See 3.8.4 Power Domains for a list of the peripherals in each power domain.

4.7 Flash Characteristics

Table 4.8. Flash Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Flash Supply voltage during write or erase	V_{FLASH}		1.71	—	3.8	V
Flash erase cycles before failure[1]	EC_{FLASH}		10,000	—	—	cycles
Flash data retention[1]	RET_{FLASH}		10	—	—	years
Program Time	t_{PROG}	one word (32-bits)	42.1	44	45.6	uSec
		average per word over 128 words	10.3	10.9	11.3	uSec
Page Erase Time	t_{PERASE}		11.4	12.9	14.4	ms
Mass Erase Time	t_{MERASE}	Erases all of User Code area	11.7	13	14.3	ms
Program Current	I_{PROG}		—	—	1.45	mA
Page Erase Current	I_{PERASE}	Page Erase	—	—	1.34	mA
Mass Erase Current	I_{MERASE}	Mass Erase	—	—	1.28	mA

Note:
1. Flash data retention information is published in the Quarterly Quality and Reliability Report.

4.8 Wake Up, Entry, and Exit times

Unless otherwise specified, these times are measured using the HFRCO at 19 MHz.

Table 4.9. Wake Up, Entry, and Exit times

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
WakeupTime from EM1	t_{EM1_WU}	Code execution from flash	—	3	—	HCLKs
		Code execution from RAM	—	1.42	—	µs
WakeupTime from EM2	t_{EM2_WU}	Code execution from flash, No Voltage Scaling	—	13.22	—	µs
		Code execution from RAM, No Voltage Scaling	—	5.15	—	µs
		Voltage scaling up one level[1]	—	37.89	—	µs
		Voltage scaling up two levels[2]	—	50.56	—	µs
WakupTime from EM3	t_{EM3_WU}	Code execution from flash, No Voltage Scaling	—	13.21	—	µs
		Code execution from RAM, No Voltage Scaling	—	5.15	—	µs
		Voltage scaling up one level[1]	—	37.90	—	µs
		Voltage scaling up two levels[2]	—	50.55	—	µs
WakeupTime from EM4	t_{EM4_WU}	Code execution from flash	—	8.81	—	ms
Entry time to EM1	t_{EM1_ENT}	Code execution from flash	—	1.29	—	µs
Entry time to EM2	t_{EM2_ENT}	Code execution from flash	—	5.23	—	µs
Entry time to EM3	t_{EM3_ENT}	Code execution from flash	—	5.23	—	µs
Entry time to EM4	t_{EM4_ENT}	Code execution from flash	—	9.96	—	µs
Voltage scaling in time in EM0[3]	t_{SCALE}	Up from VSCALE1 to VSCALE2	—	32	—	µs
		Down from VSCALE2 to VSCALE1	—	172	—	µs

Note:

1. Voltage scaling one level is between VSCALE0 and VSCALE1 or between VSCALE1 and VSCALE2.
2. Voltage scaling two levels is between VSCALE0 and VSCALE2.
3. During voltage scaling in EM0, RAM is inaccessible and processor will be halted until complete.

4.9 Boot Timing

Secure boot impacts the recovery time from all sources of device reset. In addition to the root code authentication process, which cannot be disabled or bypassed, the root code can authenticate a bootloader, and the bootloader can authenticate the application. In projects that include only an application and no bootloader, the root code can authenticate the application directly. The duration of each authentication operation depends on two factors: the computation of the associated image hash, which is proportional to the size of the image, and the verification of the image signature, which is independent of image size.

The duration for the root code to authenticate the bootloader will depend on the SE firmware version as well as on the size of the bootloader.

The duration for the bootloader to authenticate the application can depend on the size of the application.

The configurations below assume that the associated bootloader and application code images do not contain a bootloader certificate or an application certificate. Authenticating a bootloader certificate or an application certificate will extend the boot time by an additional 6 to 7 ms.

The table below provides the durations from the termination of reset until the completion of the secure boot process (start of main() function in the application image) under various conditions.

Conditions:

- VSE firmware version: 1.2.6
- Gecko Bootloader size: 13.0 kB

Timing is expected to be similar for subsequent VSE firmware versions. Refer to VSE firmware release notes for any significant changes.

Table 4.10. Boot Timing

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Boot time	t_{BOOT}	Secure boot application check disabled, no bootloader	—	14.9	—	ms
		Secure boot application check disabled, second stage bootloader check enabled[1], 50 kB application size	—	21.3	—	ms
		Secure boot application check enabled, second stage bootloader check enabled[1], 50 kB application size	—	48.4	—	ms
		Secure boot application check enabled, second stage bootloader check enabled[1], 150 kB application size	—	54.0	—	ms
		Secure boot application check enabled, second stage bootloader check enabled[1], 350 kB application size	—	65.1	—	ms

Note:

1. Timing is measured with the specified bootloader size. Actual bootloader size will impact the boot timing slightly, with a similar µs / kB ratio as application size.

4.10 Oscillators

4.10.1 High Frequency Crystal Oscillator

Unless otherwise indicated, typical conditions are: AVDD = DVDD = 3.0 V. T_A = 25 °C. Minimum and maximum values in this table represent the worst conditions across process variation, operating supply voltage range, and operating temperature range.

Table 4.11. High Frequency Crystal Oscillator

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Crystal Frequency	F_{HFXO}		—	38.4	—	MHz
Supported crystal equivalent series resistance (ESR)	ESR_{HFXO_38M4}	38.4 MHz, CL = 10 pF[1]	—	40	60	Ω
Supported range of crystal load capacitance[2]	C_{HFXO_LC}	38.4 MHz, ESR = 40 Ω	—	10	—	pF
Supply Current	I_{HFXO}		—	415	—	µA
Startup Time[3]	$T_{STARTUP}$	38.4 MHz, ESR = 40 Ohm, CL = 10 pF	—	160	—	µs
On-chip tuning cap step size[4]	SS_{HFXO}		—	0.04	—	pF

Note:

1. The crystal should have a maximum ESR less than or equal to this maximum rating.
2. Total load capacitance as seen by the crystal.
3. Startup time does not include time implemented by programmable TIMEOUTSTEADY delay.
4. The tuning step size is the effective step size when incrementing both of the tuning capacitors by one count. The step size for the each of the individual tuning capacitors is twice this value.

4.10.2 Low Frequency Crystal Oscillator

Table 4.12. Low Frequency Crystal Oscillator

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Crystal Frequency	F_{LFXO}		—	32.768	—	kHz
Supported Crystal equivalent series resistance (ESR)	ESR_{LFXO}	GAIN = 0	—	—	80	kΩ
		GAIN = 1 to 3	—	—	100	kΩ
Supported range of crystal load capacitance [1]	C_{LFXO_CL}	GAIN = 0	4	—	6	pF
		GAIN = 1	6	—	10	pF
		GAIN = 2 (see note[2])	10	—	12.5	pF
		GAIN = 3 (see note[2])	12.5	—	18	pF
Current consumption	I_{CL12p5}	ESR = 70 kOhm, CL = 12.5 pF, GAIN[3] = 2, AGC[4] = 1	—	357	—	nA
Startup Time	$T_{STARTUP}$	ESR = 70 kOhm, CL = 7 pF, GAIN[3] = 1, AGC[4] = 1	—	63	—	ms
On-chip tuning cap step size	SS_{LFXO}		—	0.26	—	pF
On-chip tuning capacitor value at minimum setting[5]	C_{LFXO_MIN}	CAPTUNE = 0	—	4	—	pF
On-chip tuning capacitor value at maximum setting[5]	C_{LFXO_MAX}	CAPTUNE = 0x4F	—	24.5	—	pF

Note:

1. Total load capacitance seen by the crystal
2. Crystals with a load capacitance of greater than 12 pF require external load capacitors.
3. In LFXO_CAL Register
4. In LFXO_CFG Register
5. The effective load capacitance seen by the crystal will be $C_{LFXO}/2$. This is because each XTAL pin has a tuning cap and the two caps will be seen in series by the crystal

4.10.3 High Frequency RC Oscillator (HFRCO)

Unless otherwise indicated, typical conditions are: AVDD = DVDD = 3.0 V. T_A = 25 °C. Minimum and maximum values in this table represent the worst conditions across process variation, operating supply voltage range, and operating temperature range.

Table 4.13. High Frequency RC Oscillator (HFRCO)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Frequency Accuracy	F_{HFRCO_ACC}	For all production calibrated frequencies	-3	—	3	%
Current consumption on all supplies [1]	I_{HFRCO}	F_{HFRCO} = 1 MHz	—	28	—	µA
		F_{HFRCO} = 2 MHz	—	28	—	µA
		F_{HFRCO} = 4 MHz	—	28	—	µA
		F_{HFRCO} = 5 MHz	—	30	—	µA
		F_{HFRCO} = 7 MHz	—	60	—	µA
		F_{HFRCO} = 10 MHz	—	66	—	µA
		F_{HFRCO} = 13 MHz	—	79	—	µA
		F_{HFRCO} = 16 MHz	—	88	—	µA
		F_{HFRCO} = 19 MHz	—	92	—	µA
		F_{HFRCO} = 20 MHz	—	105	—	µA
		F_{HFRCO} = 26 MHz	—	118	—	µA
		F_{HFRCO} = 32 MHz	—	141	—	µA
		F_{HFRCO} = 38 MHz	—	172	—	µA
		F_{HFRCO} = 80 MHz	—	289	—	µA
Clock out current for HFRCODPLL[2]	$I_{CLKOUT\_HFRCODPLL}$	FORCEEN bit of HFRCO0_CTRL = 1	—	3.0	—	µA/MHz
Startup Time[3]	$T_{STARTUP}$	FREQRANGE = 0 to 7	—	1.2	—	µs
		FREQRANGE = 8 to 15	—	0.6	—	µs

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Band Frequency Limits[4]	f_{HFRCO_BAND}	FREQRANGE = 0	3.71	—	5.24	MHz
		FREQRANGE = 1	4.39	—	6.26	MHz
		FREQRANGE = 2	5.25	—	7.55	MHz
		FREQRANGE = 3	6.22	—	9.01	MHz
		FREQRANGE = 4	7.88	—	11.6	MHz
		FREQRANGE = 5	9.9	—	14.6	MHz
		FREQRANGE = 6	11.5	—	17.0	MHz
		FREQRANGE = 7	14.1	—	20.9	MHz
		FREQRANGE = 8	16.4	—	24.7	MHz
		FREQRANGE = 9	19.8	—	30.4	MHz
		FREQRANGE = 10	22.7	—	34.9	MHz
		FREQRANGE = 11	28.6	—	44.4	MHz
		FREQRANGE = 12	33.0	—	51.0	MHz
		FREQRANGE = 13	42.2	—	64.6	MHz
		FREQRANGE = 14	48.8	—	74.8	MHz
		FREQRANGE = 15	57.6	—	87.4	MHz

Note:

1. Does not include additional clock tree current. See specifications for additional current when selected as a clock source for a particular clock multiplexer.
2. When the HFRCO is enabled for characterization using the FORCEEN bit, the total current will be the HFRCO core current plus the specified CLKOUT current. When the HFRCO is enabled on demand, the clock current may be different.
3. Hardware delay ensures settling to within ± 0.5%. Hardware also enforces this delay on a band change.
4. The frequency band limits represent the lowest and highest frequency which each band can achieve over the operating range.

4.10.4 Fast Start_Up RC Oscillator (FSRCO)

Table 4.14. Fast Start_Up RC Oscillator (FSRCO)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
FSRCO frequency	F_{FSRCO}		17.2	20	21.2	MHz

4.10.5 Low Frequency RC Oscillator (LFRCO)

Table 4.15. Low Frequency RC Oscillator (LFRCO)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Nominal oscillation frequency	F_{LFRCO}		—	32.768	—	kHz
Frequency accuracy	F_{LFRCO_ACC}		-3	—	3	%
Startup time	$t_{STARTUP}$		—	204	—	µs
Current consumption	I_{LFRCO}		—	175	—	nA

4.10.6 Ultra Low Frequency RC Oscillator

Table 4.16. Ultra Low Frequency RC Oscillator

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Oscillation Frequency	F_{ULFRCO}		0.944	1.0	1.095	kHz

4.11 GPIO Pins (3V GPIO pins)

Table 4.17. GPIO Pins (3V GPIO pins)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Leakage current	I_{LEAK_IO}	MODEx = DISABLED, IOVDD = 1.71 V	—	1.9	—	nA
		MODEx = DISABLED, IOVDD = 3.0 V	—	2.5	—	nA
		Pins other than PA00, PA03, PB00, PC03, PC04 and PD00; MODEx = DISABLED, IOVDD = 3.8 V T_A = 125 °C	—	—	200	nA
		Pins PA00, PA03, PB00, PC03, PC04 and PD00; MODEx = DISABLED, IOVDD = 3.8 V T_A = 125 °C	—	—	550	nA
Input low voltage[1]	V_{IL}	Any GPIO pin	—	—	0.3*IOVDD	V
		RESETn	—	—	0.3*DVDD	V
Input high voltage[1]	V_{IH}	Any GPIO pin	0.7*IOVDD	—	—	V
		RESETn	0.7*DVDD	—	—	V
Hysteresis of input voltage	V_{HYS}	Any GPIO pin	0.05*IOVDD	—	—	V
		RESETn	0.05*DVDD	—	—	V
Output high voltage	V_{OH}	Sourcing 20mA, IOVDD = 3.0 V	0.8 * IOVDD	—	—	V
		Sourcing 8mA, IOVDD = 1.71 V	0.6 * IOVDD	—	—	V
Output low voltage	V_{OL}	Sinking 20mA, IOVDD = 3.0 V	—	—	0.2 * IOVDD	V
		Sinking 8mA, IOVDD = 1.71 V	—	—	0.4 * IOVDD	V
GPIO rise time	T_{GPIO_RISE}	IOVDD = 3.0 V, C_{load} = 50pF, SLEWRATE = 4, 10% to 90%	—	8.4	—	ns
		IOVDD = 1.71 V, C_{load} = 50pF, SLEWRATE = 4, 10% to 90%	—	13	—	ns
GPIO fall time	T_{GPIO_FALL}	IOVDD = 3.0 V, C_{load} = 50pF, SLEWRATE = 4, 90% to 10%	—	7.1	—	ns
		IOVDD = 1.71 V, C_{load} = 50pF, SLEWRATE = 4, 90% to 10%	—	11.9	—	ns
Pull up/down resistance[2]	R_{PULL}	Any GPIO pin. Pull-up to IOVDD: MODEn = DISABLE DOUT=1. Pull-down to VSS: MODEn = WIREDORPULLDOWN DOUT = 0.	35	44	55	kΩ
		RESETn pin. Pull-up to DVDD	35	44	55	kΩ
Maximum filtered glitch width	T_{GF}	MODE = INPUT, DOUT = 1	—	27	—	ns

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
RESETn low time to ensure pin reset	T_{RESET}		100	—	—	ns

Note:

1. GPIO input thresholds are proportional to the IOVDD pin. RESETn input thresholds are proportional to DVDD.
2. GPIO pull-ups connect to IOVDD supply, pull-downs connect to VSS. RESETn pull-up connects to DVDD.

4.12 Analog to Digital Converter (IADC)

Specified at 1 Msps, ADCCLK = 10 MHz, OSR=2, unless otherwise indicated.

Table 4.18. Analog to Digital Converter (IADC)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Main analog supply	V_{AVDD}	Normal Mode	1.71	—	3.8	V
Maximum Input Range[1]	V_{IN_MAX}	Maximum allowable input voltage	0	—	AVDD	V
Full-Scale Voltage	V_{FS}	Voltage required for Full-Scale measurement	—	V_{REF} / Gain	—	V
Input Measurement Range	V_{IN}	Differential Mode - Plus and Minus inputs	$-V_{FS}$	—	$+V_{FS}$	V
		Single Ended Mode - One input tied to ground	0	—	V_{FS}	V
Input Sampling Capacitance	Cs	Analog Gain = 1x	—	1.8	—	pF
		Analog Gain = 2x	—	3.6	—	pF
		Analog Gain = 3x	—	5.4	—	pF
		Analog Gain = 4x	—	7.2	—	pF
		Analog Gain = 0.5x	—	0.9	—	pF
ADC clock frequency	f_{ADC_CLK}	Gain = 1x or 0.5x	—	—	10	MHz
		Gain = 2x	—	—	5	MHz
		Gain = 3x or 4x	—	—	2.5	MHz
Input sampling frequency	f_S		—	$f_{ADC\_CLK}/4$	—	MHz
Throughput rate	f_{SAMPLE}	f_{ADC_CLK} = 10 MHz, OSR = 2	—	—	1	Msps
		f_{ADC_CLK} = 10 MHz, OSR = 32	—	—	76.9	ksps
Current from all supplies, Continuous operation	I_{ADC_CONT}	1 Msps, OSR = 2, f_{ADC_CLK} = 10 MHz	—	290	385	µA
Current in Standby mode. ADC is not functional but can wake up in 1us.	I_{STBY}		—	16	—	µA
ADC Startup Time	$t_{startup}$	From power down state	—	5	—	µs
		From standby state	—	1	—	µs
ADC Resolution[2]	Resolution		—	12	—	bits
Differential Nonlinearity	DNL	Differential Input, OSR = 2, (No missing codes) .	-1	+/- 0.25	1.5	LSB12
Integral Nonlinearity	INL	Differential Input, OSR = 2.	-2.5	+/- 0.65	2.5	LSB12

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Effective number of bits[3]	ENOB	Differential Input. Gain = 1x, OSR = 2, f_{IN} = 10 kHz, Internal VREF=1.21V. OSR=2	10.5	11.7	—	bits
		Differential Input. Gain = 1x, OSR = 32, f_{IN} = 2.5 kHz, Internal VREF = 1.21 V.	—	13.5	—	bits
		Differential Input. Gain = 1x, OSR = 32, f_{IN} = 2.5 kHz, External VREF = 1.25 V.	—	14.3	—	bits
Signal to Noise + Distortion Ratio[3]	SNDR	Differential Input. Gain=1x, OSR = 2, f_{IN} = 10 kHz, Internal VREF=1.21V	65	72.3	—	dB
		Differential Input. Gain=2x, OSR = 2, f_{IN} = 10 kHz, Internal VREF=1.21V	—	72.3	—	dB
		Differential Input. Gain=4x, OSR = 2, f_{IN} = 10 kHz, Internal VREF=1.21V	—	68.8	—	dB
		Differential Input. Gain=0.5x, OSR = 2, f_{IN} = 10 kHz, Internal VREF=1.21V	—	72.5	—	dB
Total Harmonic Distortion	THD	Differential Input. Gain=1x, OSR = 2, f_{IN} = 10 kHz, Internal VREF=1.21V	—	-80.8	-70	dB
Spurious-Free Dynamic Range	SFDR	Differential Input. Gain=1x, OSR = 2, f_{IN} = 10 kHz, Internal VREF=1.21V	72	86.5	—	dB
Common Mode Rejection Ratio	CMRR	Normal Mode. DC to 100 Hz	—	87.0	—	dB
		Normal Mode. AC high frequency	—	68.6	—	dB
Power Supply Rejection Ratio	PSRR	DC to 100 Hz	—	80.4	—	dB
		AC high frequency, using VREF pad.	—	33.4	—	dB
		AC high frequency, using internal VBGR.	—	65.2	—	dB
Gain Error	GE	GAIN=1 and 0.5, using external VREF	-0.3	0.069	0.3	%
		GAIN=2, using external VREF	-0.4	0.151	0.4	%
		GAIN=3, using external VREF	-0.7	0.186	0.7	%
		GAIN=4, using external VREF	-1.1	0.227	1.1	%
		Internal VREF[4], all GAIN settings	-1.5	0.023	1.5	%
Offset Error	OFFSET	GAIN=1 and 0.5, Differential Input	-3	0.27	3	LSB12
		GAIN=2, Differential Input	-4	0.27	4	LSB12
		GAIN=3, Differential Input	-4	0.25	4	LSB12
		GAIN=4, Differential Input	-4	0.29	4	LSB12

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
External reference voltage range[1]	V_{EVREF}		1.0	—	AVDD	V
Internal Reference voltage	V_{IVREF}		—	1.21	—	V

Note:

1. When inputs are routed to external GPIO pins, the maximum pin voltage is limited to the lower of the IOVDD and AVDD supplies.
2. ADC output resolution depends on the OSR and digital averaging settings. With no digital averaging, ADC output resolution is 12 bits at OSR=2, 13 bits at OSR = 4, 14 bits at OSR = 8, 15 bits at OSR = 16, 16 bits at OSR = 32 and 17 bits at OSR = 64. Digital averaging has a similar impact on ADC output resolution. See the product reference manual for additional details.
3. The relationship between ENOB and SNDR is specified according to the equation: ENOB = (SNDR - 1.76) / 6.02.
4. Includes error from internal VREF drift.

4.13 Temperature Sensor

Table 4.19. Temperature Sensor

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Temperature sensor range[1]	T_{RANGE}		-40	—	125	°C
Temperature sensor resolution	$T_{RESOLUTION}$		—	0.25	—	°C
Measurement noise (RMS)	T_{NOISE}	Single measurement	—	0.6	—	°C
		16-sample average (TEMPAVGNUM = 0)	—	0.17	—	°C
		64-sample average (TEMPAVGNUM = 1)	—	0.12	—	°C
Temperature offset	T_{OFF}	Mean error of uncorrected output across full temperature range	—	3.14	—	°C
Temperature sensor accuracy[2] [3]	T_{ACC}	Direct output accuracy after mean error (T_{OFF}) removed	-3	—	3	°C
		After linearization in software, no calibration	-2	—	2	°C
		After linearization in software, with single-temperature calibration at 25 °C[4]	-1.5	—	1.5	°C
Measurement interval	t_{MEAS}		—	250	—	ms

Note:

1. The sensor reports absolute die temperature in °K. All specifications are in °C to match the units of the specified product temperature range.
2. Error is measured as the deviation of the mean temperature reading from the expected die temperature. Accuracy numbers represent statistical minimum and maximum using ± 4 standard deviations of measured error.
3. The raw output of the temperature sensor is a predictable curve. It can be linearized with a polynomial function for additional accuracy.
4. Assuming calibration accuracy of ± 0.25 °C.

4.14 Brown Out Detectors

4.14.1 DVDD BOD

BOD thresholds on DVDD in EM0 and EM1 only, unless otherwise noted. Typical conditions are at T_A = 25 °C. Minimum and maximum values in this table represent the worst conditions across process variation, operating supply voltage range, and operating temperature range.

Table 4.20. DVDD BOD

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
BOD threshold	V_{DVDD_BOD}	Supply Rising	—	1.64	1.71	V
		Supply Falling	1.62	1.65	—	V
BOD response time	$t_{DVDD\_BOD\_DELAY}$	Supply dropping at 100 mV/µs slew rate[1]	—	0.95	—	µs
BOD hysteresis	$V_{DVDD\_BOD\_HYST}$		—	20	—	mV

Note:
1. If the supply slew rate exceeds the specified slew rate, the BOD may trip later than expected (at a threshold below the minimum specified threshold), or the BOD may not trip at all (e.g., if the supply ramps down and then back up at a very fast rate)

4.14.2 LE DVDD BOD

BOD thresholds on DVDD pin for low energy modes EM2 to EM4, unless otherwise noted.

Table 4.21. LE DVDD BOD

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
BOD threshold	$V_{DVDD\_LE\_BOD}$	Supply Falling	1.5	—	1.71	V
BOD response time	$t_{DVDD\_LE\_BOD\_DELAY}$	Supply dropping at 2 mV/µs slew rate[1]	—	50	—	µs
BOD hysteresis	$V_{DVDD\_LE\_BOD\_HYST}$		—	20	—	mV

Note:
1. If the supply slew rate exceeds the specified slew rate, the BOD may trip later than expected (at a threshold below the minimum specified threshold), or the BOD may not trip at all (e.g., if the supply ramps down and then back up at a very fast rate)

4.14.3 AVDD and IOVDD BODs

BOD thresholds for AVDD BOD and IOVDD BOD. Available in all energy modes.

Table 4.22. AVDD and IOVDD BODs

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
BOD threshold	V_{BOD}	Supply falling	1.45	—	1.71	V
BOD response time	t_{BOD_DELAY}	Supply dropping at 2 mV/µs slew rate[1]	—	50	—	µs
BOD hysteresis	V_{BOD_HYST}		—	20	—	mV

Note:

1. If the supply slew rate exceeds the specified slew rate, the BOD may trip later than expected (at a threshold below the minimum specified threshold), or the BOD may not trip at all (e.g., if the supply ramps down and then back up at a very fast rate)

4.15 PDM Timing Specifications

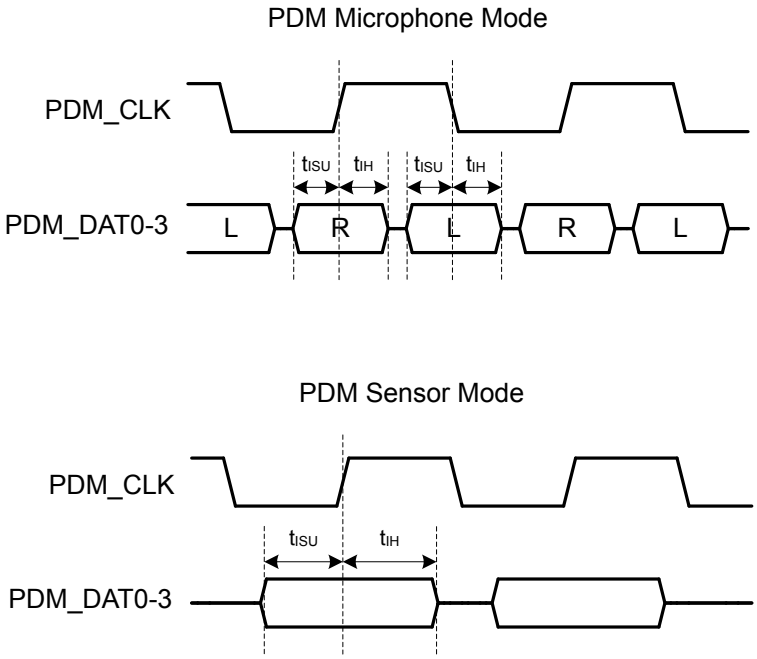

Figure 4.3. PDM Timing Diagrams

4.15.1 Pulse Density Modulator (PDM), Common DBUS

Timing specifications are for all PDM signals routed to the same DBUS (DBUSAB or DBUSCD), though routing to the same GPIO port is the optimal configuration. C_{LOAD} < 20 pF. System voltage scaling = VSCALE1 or VSCALE2. All GPIO set to slew rate = 6. Data delay (PDM_CFG1_DLYMUXSEL) = 0.

Table 4.23. Pulse Density Modulator (PDM), Common DBUS

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
PDM_CLK frequency during data transfer	F_{PDM_CLK}	Microphone mode	—	—	5	MHz
		Sensor mode	—	—	20	MHz
PDM_CLK duty cycle	DC_{PDM_CLK}		47.5	—	52.5	%
PDM_CLK rise time	t_R		—	—	5.5	ns
PDM_CLK fall time	t_F		—	—	5.5	ns
Input setup time	t_{ISU}	Microphone mode	30	—	—	ns
		Sensor mode	20	—	—	ns
Input hold time	t_{IH}		3	—	—	ns

4.16 USART SPI Main Timing

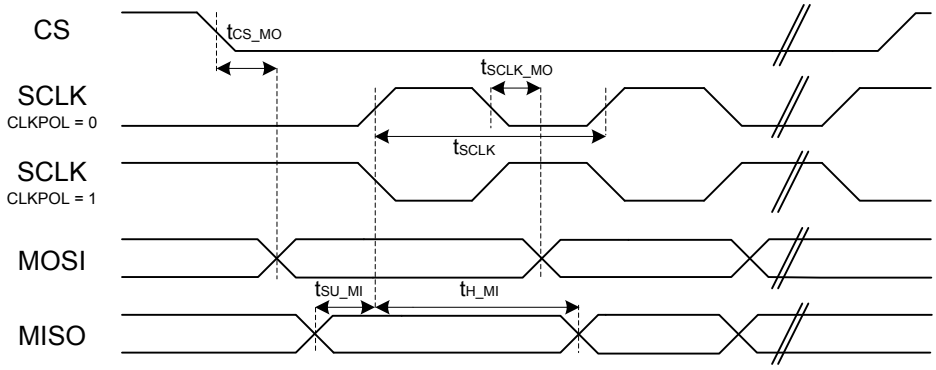

Figure 4.4. SPI Main Timing (SMSDELAY = 0)

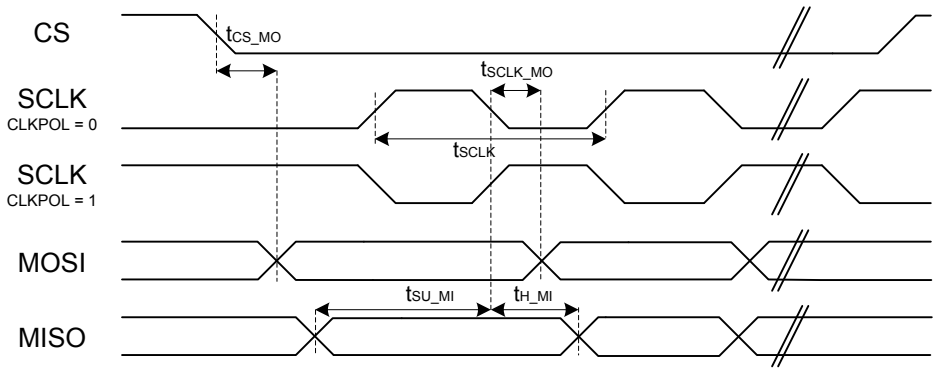

Figure 4.5. SPI Main Timing (SMSDELAY = 1)

4.16.1 USART SPI Main Timing, Voltage Scaling = VSCALE2

Timing specifications are for all SPI signals routed to the same DBUS (DBUSAB or DBUSCD). All GPIO set to slew rate = 6.

Table 4.24. USART SPI Main Timing, Voltage Scaling = VSCALE2

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK period [1] [2] [3]	t_{SCLK}		$2*t_{PCLK}$	—	—	ns
CS to MOSI [1] [2]	t_{CS_MO}		-22	—	22.5	ns
SCLK to MOSI [1] [2]	t_{SCLK_MO}		-14.5	—	14.5	ns
MISO setup time [1] [2]	t_{SU_MI}	IOVDD = 1.62 V	38.5	—	—	ns
		IOVDD = 3.0 V	28.5	—	—	ns
MISO hold time [1] [2]	t_{H_MI}		-8.5	—	—	ns

Note:
1. Applies for both CLKPHA = 0 and CLKPHA = 1.
2. Measurement done with 8 pF output loading at 10% and 90% of V_{DD}.
3. t_{PCLK} is one period of the selected PCLK.

4.16.2 USART SPI Main Timing, Voltage Scaling = VSCALE1

Timing specifications are for all SPI signals routed to the same DBUS (DBUSAB or DBUSCD). All GPIO set to slew rate = 6.

Table 4.25. USART SPI Main Timing, Voltage Scaling = VSCALE1

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK period [1] [2] [3]	t_{SCLK}		$2*t_{PCLK}$	—	—	ns
CS to MOSI [1] [2]	t_{CS_MO}		-33	—	34.5	ns
SCLK to MOSI [1] [2]	t_{SCLK_MO}		-15	—	26	ns
MISO setup time [1] [2]	t_{SU_MI}	IOVDD = 1.62 V	47	—	—	ns
		IOVDD = 3.0 V	39	—	—	ns
MISO hold time [1] [2]	t_{H_MI}		-9.5	—	—	ns

Note:
1. Applies for both CLKPHA = 0 and CLKPHA = 1.
2. Measurement done with 8 pF output loading at 10% and 90% of V_{DD}.
3. t_{PCLK} is one period of the selected PCLK.

4.17 USART SPI Secondary Timing

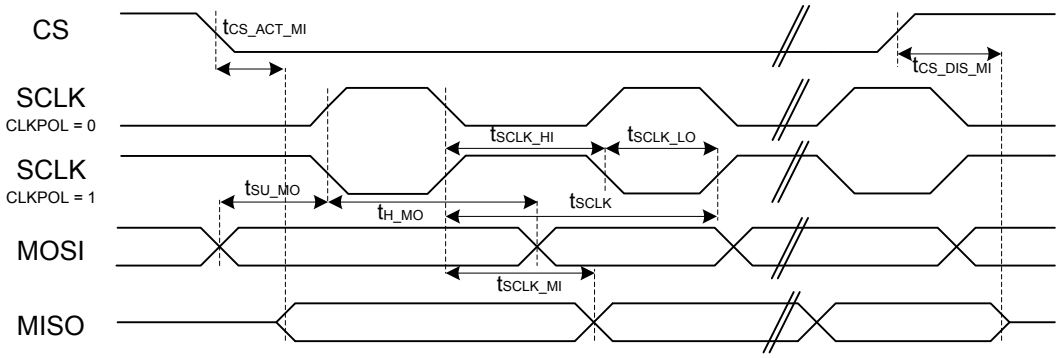

Figure 4.6. SPI Secondary Timing

4.17.1 USART SPI Secondary Timing, Voltage Scaling = VSCALE2

Timing specifications are for all SPI signals routed to the same DBUS (DBUSAB or DBUSCD). All GPIO set to slew rate = 6.

Table 4.26. USART SPI Secondary Timing, Voltage Scaling = VSCALE2

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK period [1] [2] [3]	t_{SCLK}		6*t_{PCLK}	—	—	ns
SCLK high time [1] [2] [3]	t_{SCLK_HI}		2.5*t_{PCLK}	—	—	ns
SCLK low time [1] [2] [3]	t_{SCLK_LO}		2.5*t_{PCLK}	—	—	ns
CS active to MISO [1] [2]	$t_{CS\_ACT\_MI}$		25	—	47.5	ns
CS disable to MISO [1] [2]	$t_{CS\_DIS\_MI}$		19.5	—	38.5	ns
MOSI setup time [1] [2]	t_{SU_MO}		4.5	—	—	ns
MOSI hold time [1] [2] [3]	t_{H_MO}		5	—	—	ns
SCLK to MISO [1] [2] [3]	t_{SCLK_MI}		22 + 1.5*t_{PCLK}	—	33.5 + 2.5*t_{PCLK}	ns

Note:
1. Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0).
2. Measurement done with 8 pF output loading at 10% and 90% of V_{DD} (figure shows 50% of V_{DD}).
3. t_{PCLK} is one period of the selected PCLK.

4.17.2 USART SPI Secondary Timing, Voltage Scaling = VSCALE1

Timing specifications are for all SPI signals routed to the same DBUS (DBUSAB or DBUSCD). All GPIO set to slew rate = 6.

Table 4.27. USART SPI Secondary Timing, Voltage Scaling = VSCALE1

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK period [1] [2] [3]	t_{SCLK}		$6*t_{PCLK}$	—	—	ns
SCLK high time [1] [2] [3]	t_{SCLK_HI}		$2.5*t_{PCLK}$	—	—	ns
SCLK low time [1] [2] [3]	t_{SCLK_LO}		$2.5*t_{PCLK}$	—	—	ns
CS active to MISO [1] [2]	$t_{CS\_ACT\_MI}$		30.5	—	57.5	ns
CS disable to MISO [1] [2]	$t_{CS\_DIS\_MI}$		25	—	55	ns
MOSI setup time [1] [2]	t_{SU_MO}		7.5	—	—	ns
MOSI hold time [1] [2] [3]	t_{H_MO}		8.5	—	—	ns
SCLK to MISO [1] [2] [3]	t_{SCLK_MI}		$24.5 + 1.5*t_{PCLK}$	—	$45.5 + 2.5*t_{PCLK}$	ns

Note:

1. Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0).
2. Measurement done with 8 pF output loading at 10% and 90% of V_{DD} (figure shows 50% of V_{DD}).
3. t_{PCLK} is one period of the selected PCLK.

4.18 I2C Electrical Specifications

4.18.1 I2C Standard-mode (Sm)

CLHR set to 0 in the I2Cn_CTRL register.

Table 4.28. I2C Standard-mode (Sm)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCL clock frequency[1]	f_{SCL}		0	—	100	kHz
SCL clock low time	t_{LOW}		4.7	—	—	µs
SCL clock high time	t_{HIGH}		4	—	—	µs
SDA set-up time	t_{SU_DAT}		250	—	—	ns
SDA hold time	t_{HD_DAT}		0	—	—	ns
Repeated START condition set-up time	t_{SU_STA}		4.7	—	—	µs
Repeated START condition hold time	t_{HD_STA}		4.0	—	—	µs
STOP condition set-up time	t_{SU_STO}		4.0	—	—	µs
Bus free time between a STOP and START condition	t_{BUF}		4.7	—	—	µs

Note:

1. The maximum SCL clock frequency listed is assuming that an arbitrary clock frequency is available. The maximum attainable SCL clock frequency may be slightly less using the HFXO or HFRCO due to the limited frequencies available. The CLKDIV should be set to a value that keeps the SCL clock frequency below the max value listed.

4.18.2 I2C Fast-mode (Fm)

CLHR set to 1 in the I2Cn_CTRL register.

Table 4.29. I2C Fast-mode (Fm)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCL clock frequency[1]	f_{SCL}		0	—	400	kHz
SCL clock low time	t_{LOW}		1.3	—	—	µs
SCL clock high time	t_{HIGH}		0.6	—	—	µs
SDA set-up time	t_{SU_DAT}		100	—	—	ns
SDA hold time	t_{HD_DAT}		0	—	—	ns
Repeated START condition set-up time	t_{SU_STA}		0.6	—	—	µs
Repeated START condition hold time	t_{HD_STA}		0.6	—	—	µs
STOP condition set-up time	t_{SU_STO}		0.6	—	—	µs
Bus free time between a STOP and START condition	t_{BUF}		1.3	—	—	µs

Note:

1. The maximum SCL clock frequency listed is assuming that an arbitrary clock frequency is available. The maximum attainable SCL clock frequency may be slightly less using the HFXO or HFRCO due to the limited frequencies available. The CLKDIV should be set to a value that keeps the SCL clock frequency below the max value listed.

4.18.3 I2C Fast-mode Plus (Fm+)

CLHR set to 1 in the I2Cn_CTRL register.

Table 4.30. I2C Fast-mode Plus (Fm+)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCL clock frequency[1]	f_{SCL}		0	—	1000	kHz
SCL clock low time	t_{LOW}		0.5	—	—	µs
SCL clock high time	t_{HIGH}		0.26	—	—	µs
SDA set-up time	t_{SU_DAT}		50	—	—	ns
SDA hold time	t_{HD_DAT}		0	—	—	ns
Repeated START condition set-up time	t_{SU_STA}		0.26	—	—	µs
Repeated START condition hold time	t_{HD_STA}		0.26	—	—	µs
STOP condition set-up time	t_{SU_STO}		0.26	—	—	µs
Bus free time between a STOP and START condition	t_{BUF}		0.5	—	—	µs

Note:

1. The maximum SCL clock frequency listed is assuming that an arbitrary clock frequency is available. The maximum attainable SCL clock frequency may be slightly less using the HFXO or HFRCO due to the limited frequencies available. The CLKDIV should be set to a value that keeps the SCL clock frequency below the max value listed.

4.19 Typical Performance Curves

Typical performance curves indicate typical characterized performance under the stated conditions.

4.19.1 Supply Current

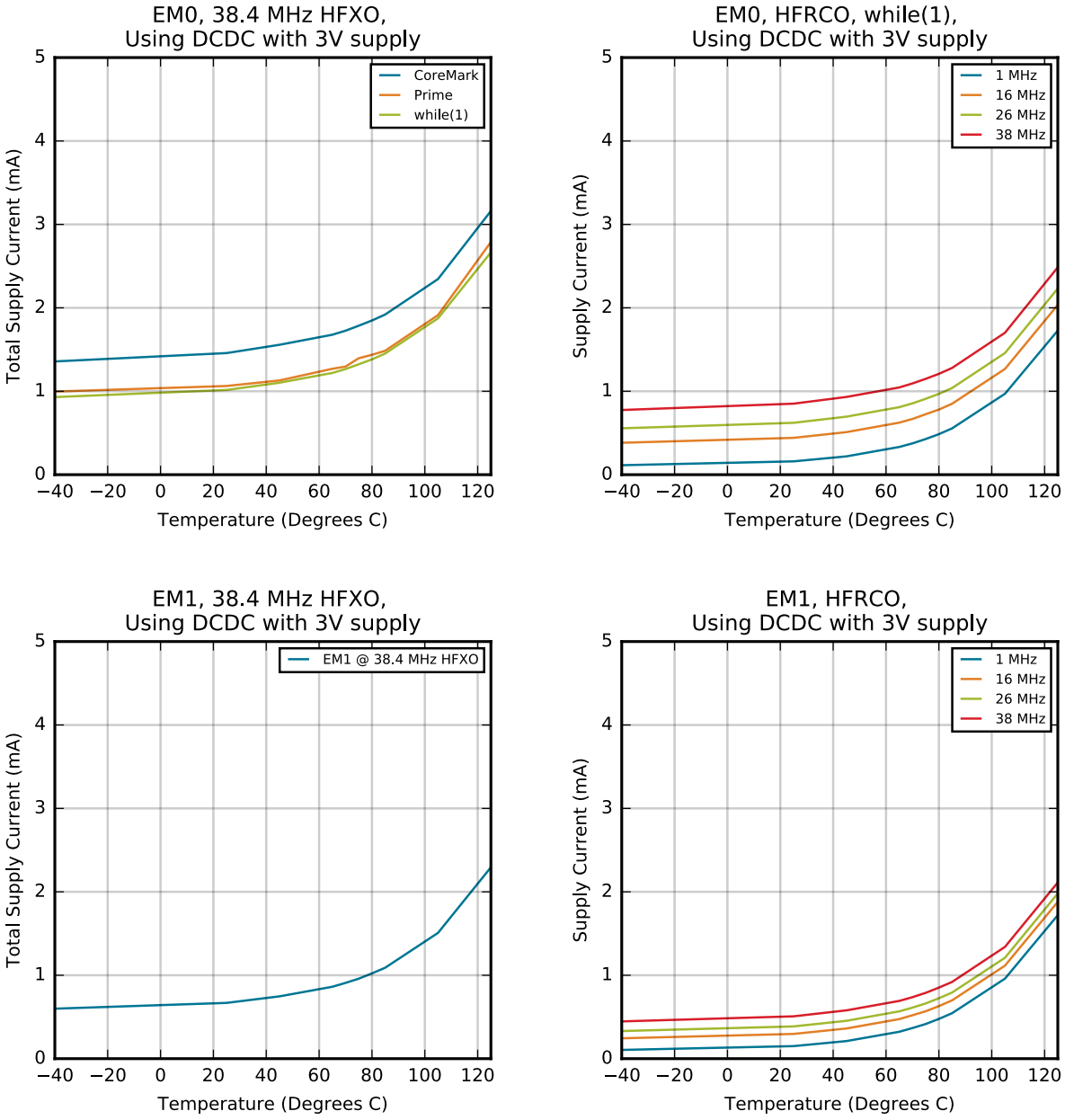

Figure 4.7. EM0 and EM1 Typical Supply Current vs. Temperature

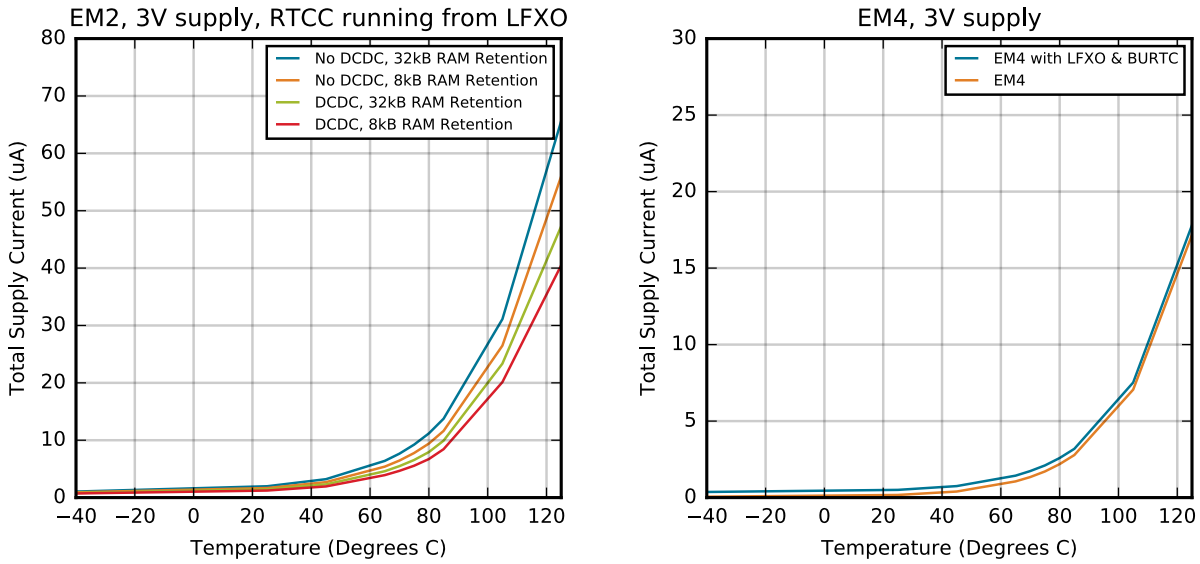

Figure 4.8. EM2 and EM4 Typical Supply Current vs. Temperature

4.19.2 DC-DC Converter

Performance characterized with Samsung CIG22H2R2MNE (L_{DCDC} = 2.2 uH) and Samsung CL10B475KQ8NQNC (C_{DCDC} = 4.7 uF)

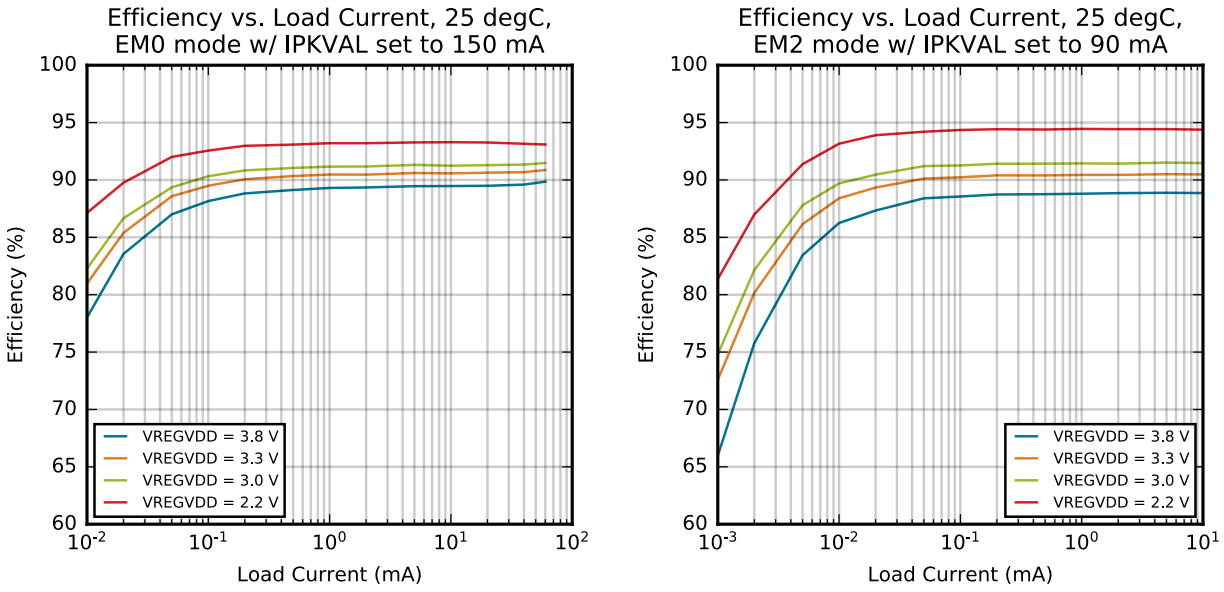

Figure 4.9. DC-DC Efficiency

4.19.3 IADC

Typical performance is shown using 10 MHz ADC clock for fastest sampling speed and adjusting oversampling ratio (OSR).

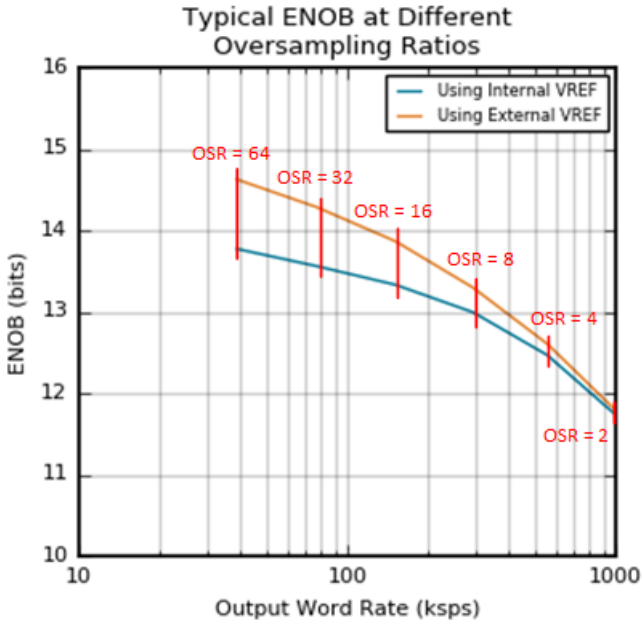

Figure 4.10. Typical ENOB vs. Oversampling Ratio

5. Typical Connections

5.1 Power

Typical power supply connections are shown in the following figures.

Note: AVDD and IOVDD supply connections are flexible. They may be connected in other configurations or to external supplies as long as the supply limits described in 4.1 Electrical Characteristics are met.

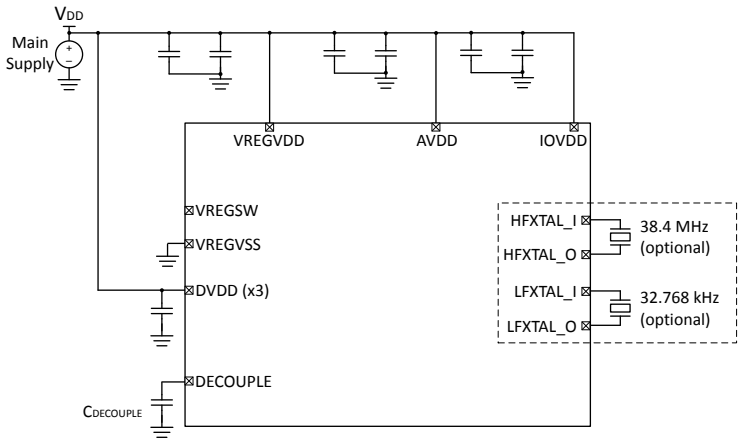

Figure 5.1. EFM32PG22 Typical Application Circuit: Direct Supply Configuration without DCDC

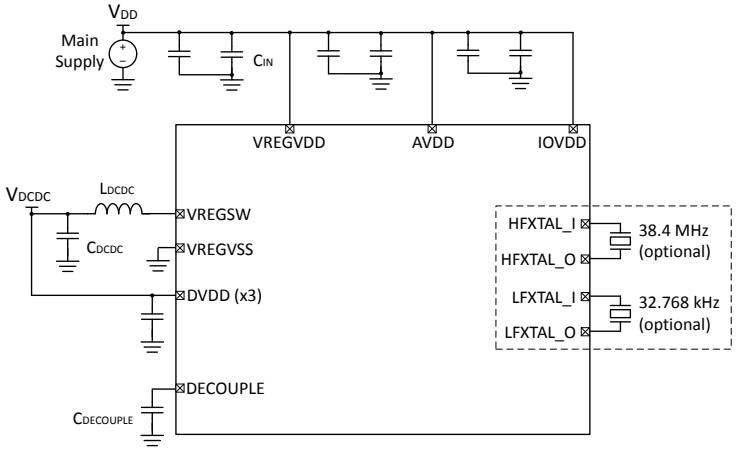

Figure 5.2. EFM32PG22 Typical Application Circuit: DCDC Configuration, AVDD and IOVDD from main supply

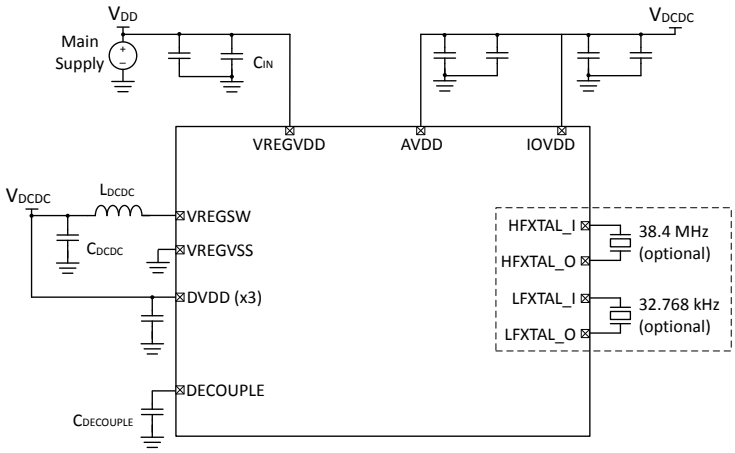

Figure 5.3. EFM32PG22 Typical Application Circuit: DCDC Configuration, AVDD and IOVDD from DCDC output

5.2 Other Connections

Other components or connections may be required to meet the system-level requirements. Application Note AN0002.2 contains detailed information on these connections. Application Notes can be accessed on the Silicon Labs website (www.silabs.com/32bit-appnotes).

6. Pin Definitions

6.1 QFN32 Device Pinout

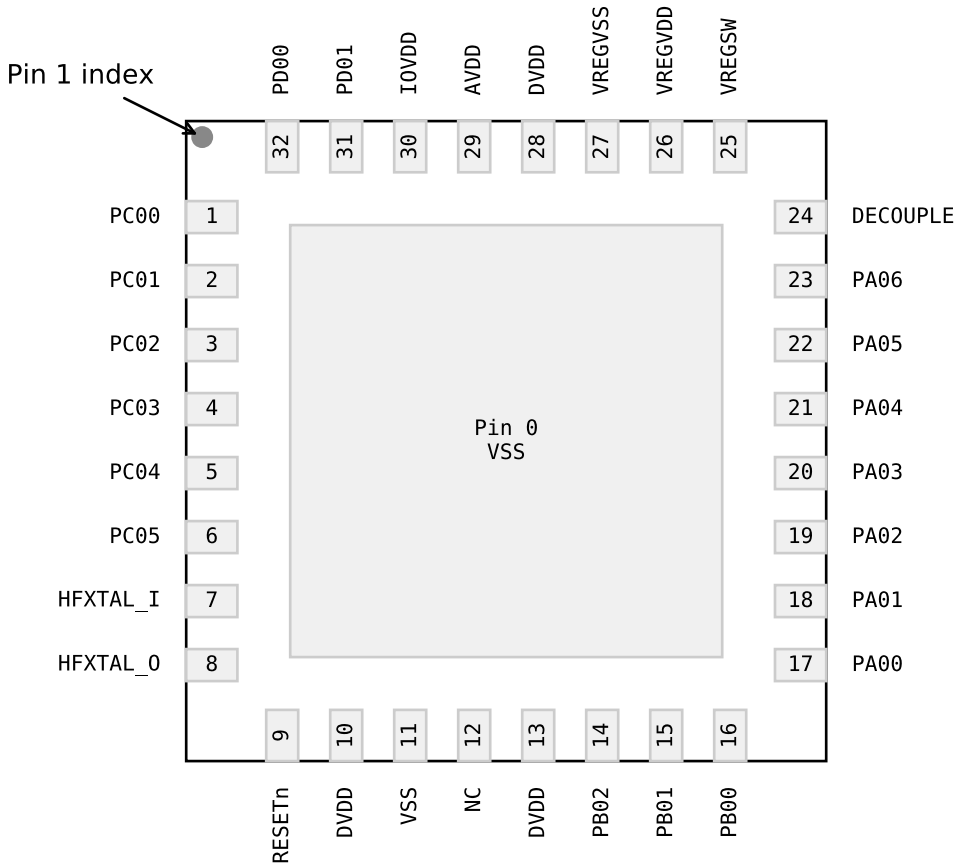

Figure 6.1. QFN32 Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see 6.3 Alternate Function Table, 6.4 Analog Peripheral Connectivity, and 6.5 Digital Peripheral Connectivity.

Table 6.1. QFN32 Device Pinout

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PC00	1	GPIO	PC01	2	GPIO
PC02	3	GPIO	PC03	4	GPIO
PC04	5	GPIO	PC05	6	GPIO
HFXTAL_I	7	High Frequency Crystal Input	HFXTAL_O	8	High Frequency Crystal Output

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
RESETn	9	Reset Pin. The RESETn pin is internally pulled up to DVDD.	DVDD	10	Digital power supply
VSS	11	Ground	NC	12	No-Connect
DVDD	13	Digital power supply	PB02	14	GPIO
PB01	15	GPIO	PB00	16	GPIO
PA00	17	GPIO	PA01	18	GPIO
PA02	19	GPIO	PA03	20	GPIO
PA04	21	GPIO	PA05	22	GPIO
PA06	23	GPIO	DECOUPLE	24	Decouple outputput for on-chip voltage regulator. An external decoupling capacitor is required at this pin.
VREGSW	25	DCDC regulator switching node	VREGVDD	26	DCDC regulator input supply
VREGVSS	27	DCDC ground	DVDD	28	Digital power supply
AVDD	29	Analog power supply	IOVDD	30	I/O power supply
PD01	31	GPIO	PD00	32	GPIO

6.2 QFN40 Device Pinout

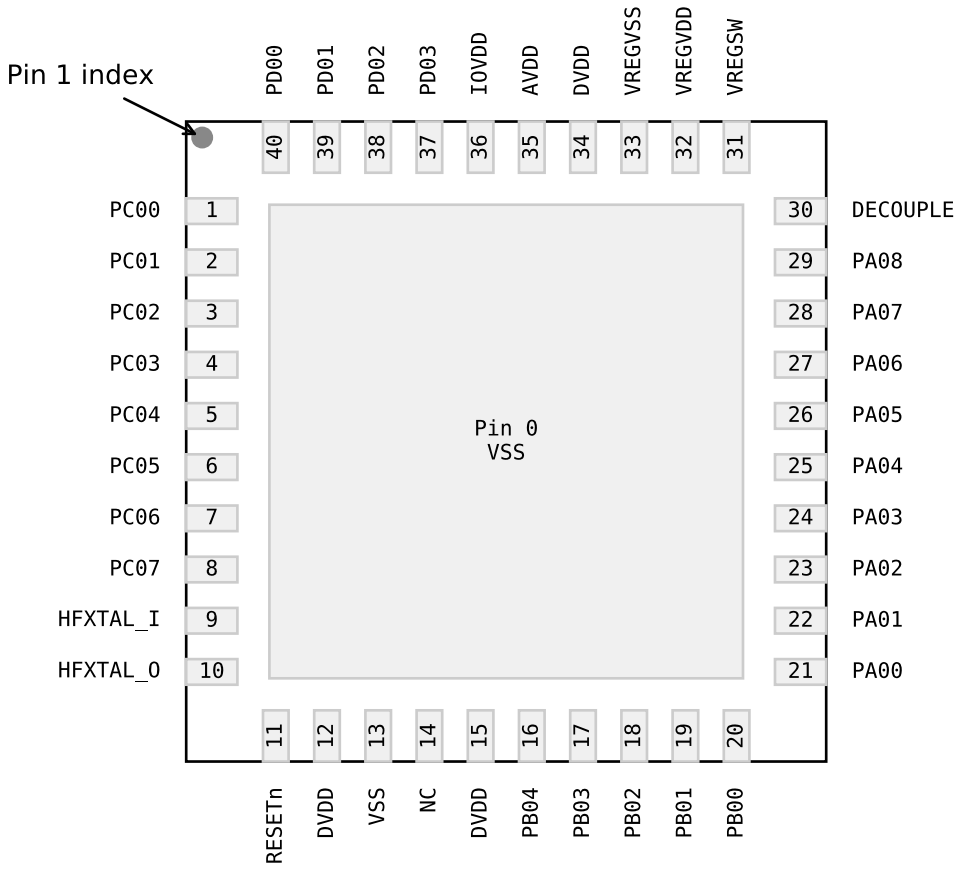

Figure 6.2. QFN40 Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see 6.3 Alternate Function Table, 6.4 Analog Peripheral Connectivity, and 6.5 Digital Peripheral Connectivity.

Table 6.2. QFN40 Device Pinout

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PC00	1	GPIO	PC01	2	GPIO
PC02	3	GPIO	PC03	4	GPIO
PC04	5	GPIO	PC05	6	GPIO
PC06	7	GPIO	PC07	8	GPIO
HFXTAL_I	9	High Frequency Crystal Input	HFXTAL_O	10	High Frequency Crystal Output
RESETn	11	Reset Pin. The RESETn pin is internally pulled up to DVDD.	DVDD	12	Digital power supply

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
VSS	13	Ground	NC	14	No-Connect
DVDD	15	Digital power supply	PB04	16	GPIO
PB03	17	GPIO	PB02	18	GPIO
PB01	19	GPIO	PB00	20	GPIO
PA00	21	GPIO	PA01	22	GPIO
PA02	23	GPIO	PA03	24	GPIO
PA04	25	GPIO	PA05	26	GPIO
PA06	27	GPIO	PA07	28	GPIO
PA08	29	GPIO	DECOUPLE	30	Decouple outputput for on-chip voltage regulator. An external decoupling capacitor is required at this pin.
VREGSW	31	DCDC regulator switching node	VREGVDD	32	DCDC regulator input supply
VREGVSS	33	DCDC ground	DVDD	34	Digital power supply
AVDD	35	Analog power supply	IOVDD	36	I/O power supply
PD03	37	GPIO	PD02	38	GPIO
PD01	39	GPIO	PD00	40	GPIO

6.3 Alternate Function Table

A wide selection of alternate functionality is available for multiplexing to various pins. The following table shows GPIO pins with support for dedicated functions across the different package options.

Table 6.3. GPIO Alternate Function Table

GPIO	Alternate Functions	QFN40 Package[2]	QFN32 Package[1]
PC00	GPIO.EM4WU6	Yes	Yes
PA03	GPIO.TRACEDATA0	Yes	Yes
	GPIO.SWV	Yes	Yes
	GPIO.TDO	Yes	Yes
PB01	GPIO.EM4WU3	Yes	Yes
PD00	LFXO.LFXTAL_O	Yes	Yes
PA00	IADC0.VREFP	Yes	Yes
PD01	LFXO.LFXTAL_I	Yes	Yes
	LFXO.LF_EXTCLK	Yes	Yes
PC05	GPIO.EM4WU7	Yes	Yes
PA02	GPIO.SWDIO	Yes	Yes
PD02	GPIO.EM4WU9	Yes	
PA05	GPIO.EM4WU0	Yes	Yes
PA01	GPIO.SWCLK	Yes	Yes
PA04	GPIO.TRACECLK	Yes	Yes
	GPIO.TDI	Yes	Yes
PC07	GPIO.EM4WU8	Yes	
PB03	GPIO.EM4WU4	Yes	

Note:

1. QFN32 Package includes OPNs EFM32PG22C200F128IM32-C, EFM32PG22C200F256IM32-C, EFM32PG22C200F512IM32-C, and EFM32PG22C200F64IM32-C
2. QFN40 Package includes OPNs EFM32PG22C200F128IM40-C, EFM32PG22C200F256IM40-C, EFM32PG22C200F512IM40-C, and EFM32PG22C200F64IM40-C

6.4 Analog Peripheral Connectivity

Many analog resources are routable and can be connected to numerous GPIO's. The table below indicates which peripherals are available on each GPIO port. When a differential connection is being used Positive inputs are restricted to the EVEN pins and Negative inputs are restricted to the ODD pins. When a single ended connection is being used positive input is available on all pins. See the device Reference Manual for more details on the ABUS and analog peripherals. Note that some functions may not be available on all device variants.

Table 6.4. ABUS Routing Table

Peripheral	Signal	PA		PB		PC		PD	
		EVEN	ODD	EVEN	ODD	EVEN	ODD	EVEN	ODD
IADC0	ANA_NEG	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	ANA_POS	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes

6.5 Digital Peripheral Connectivity

Many digital resources are routable and can be connected to numerous GPIO's. The table below indicates which peripherals are available on each GPIO port. Note that some functions may not be available on all device variants.

Table 6.5. DBUS Routing Table

Peripheral.Resource	PORT			
	PA	PB	PC	PD
CMU.CLKIN0			Available	Available
CMU.CLKOUT0			Available	Available
CMU.CLKOUT1			Available	Available
CMU.CLKOUT2	Available	Available		
EUART0.CTS	Available	Available	Available	Available
EUART0.RTS	Available	Available	Available	Available
EUART0.RX	Available	Available	Available	Available
EUART0.TX	Available	Available	Available	Available
I2C0.SCL	Available	Available	Available	Available
I2C0.SDA	Available	Available	Available	Available
I2C1.SCL			Available	Available
I2C1.SDA			Available	Available
LETIMER0.OUT0	Available	Available		
LETIMER0.OUT1	Available	Available		
PDM.CLK	Available	Available	Available	Available
PDM.DAT0	Available	Available	Available	Available
PDM.DAT1	Available	Available	Available	Available
PRS.ASYNCH0	Available	Available		
PRS.ASYNCH1	Available	Available		
PRS.ASYNCH2	Available	Available		
PRS.ASYNCH3	Available	Available		
PRS.ASYNCH4	Available	Available		
PRS.ASYNCH5	Available	Available		
PRS.ASYNCH6			Available	Available
PRS.ASYNCH7			Available	Available
PRS.ASYNCH8			Available	Available
PRS.ASYNCH9			Available	Available
PRS.ASYNCH10			Available	Available
PRS.ASYNCH11			Available	Available
PRS.SYNCH0	Available	Available	Available	Available
PRS.SYNCH1	Available	Available	Available	Available

Peripheral.Resource	PORT			
	PA	PB	PC	PD
PRS.SYNCH2	Available	Available	Available	Available
PRS.SYNCH3	Available	Available	Available	Available
TIMER0.CC0	Available	Available	Available	Available
TIMER0.CC1	Available	Available	Available	Available
TIMER0.CC2	Available	Available	Available	Available
TIMER0.CDTI0	Available	Available	Available	Available
TIMER0.CDTI1	Available	Available	Available	Available
TIMER0.CDTI2	Available	Available	Available	Available
TIMER1.CC0	Available	Available	Available	Available
TIMER1.CC1	Available	Available	Available	Available
TIMER1.CC2	Available	Available	Available	Available
TIMER1.CDTI0	Available	Available	Available	Available
TIMER1.CDTI1	Available	Available	Available	Available
TIMER1.CDTI2	Available	Available	Available	Available
TIMER2.CC0	Available	Available		
TIMER2.CC1	Available	Available		
TIMER2.CC2	Available	Available		
TIMER2.CDTI0	Available	Available		
TIMER2.CDTI1	Available	Available		
TIMER2.CDTI2	Available	Available		
TIMER3.CC0			Available	Available
TIMER3.CC1			Available	Available
TIMER3.CC2			Available	Available
TIMER3.CDTI0			Available	Available
TIMER3.CDTI1			Available	Available
TIMER3.CDTI2			Available	Available
TIMER4.CC0	Available	Available		
TIMER4.CC1	Available	Available		
TIMER4.CC2	Available	Available		
TIMER4.CDTI0	Available	Available		
TIMER4.CDTI1	Available	Available		
TIMER4.CDTI2	Available	Available		
USART0.CLK	Available	Available	Available	Available
USART0.CS	Available	Available	Available	Available
USART0.CTS	Available	Available	Available	Available
USART0.RTS	Available	Available	Available	Available

Peripheral.Resource	PORT			
	PA	PB	PC	PD
USART0.RX	Available	Available	Available	Available
USART0.TX	Available	Available	Available	Available
USART1.CLK	Available	Available		
USART1.CS	Available	Available		
USART1.CTS	Available	Available		
USART1.RTS	Available	Available		
USART1.RX	Available	Available		
USART1.TX	Available	Available		

7. QFN32 Package Specifications

7.1 QFN32 Package Dimensions

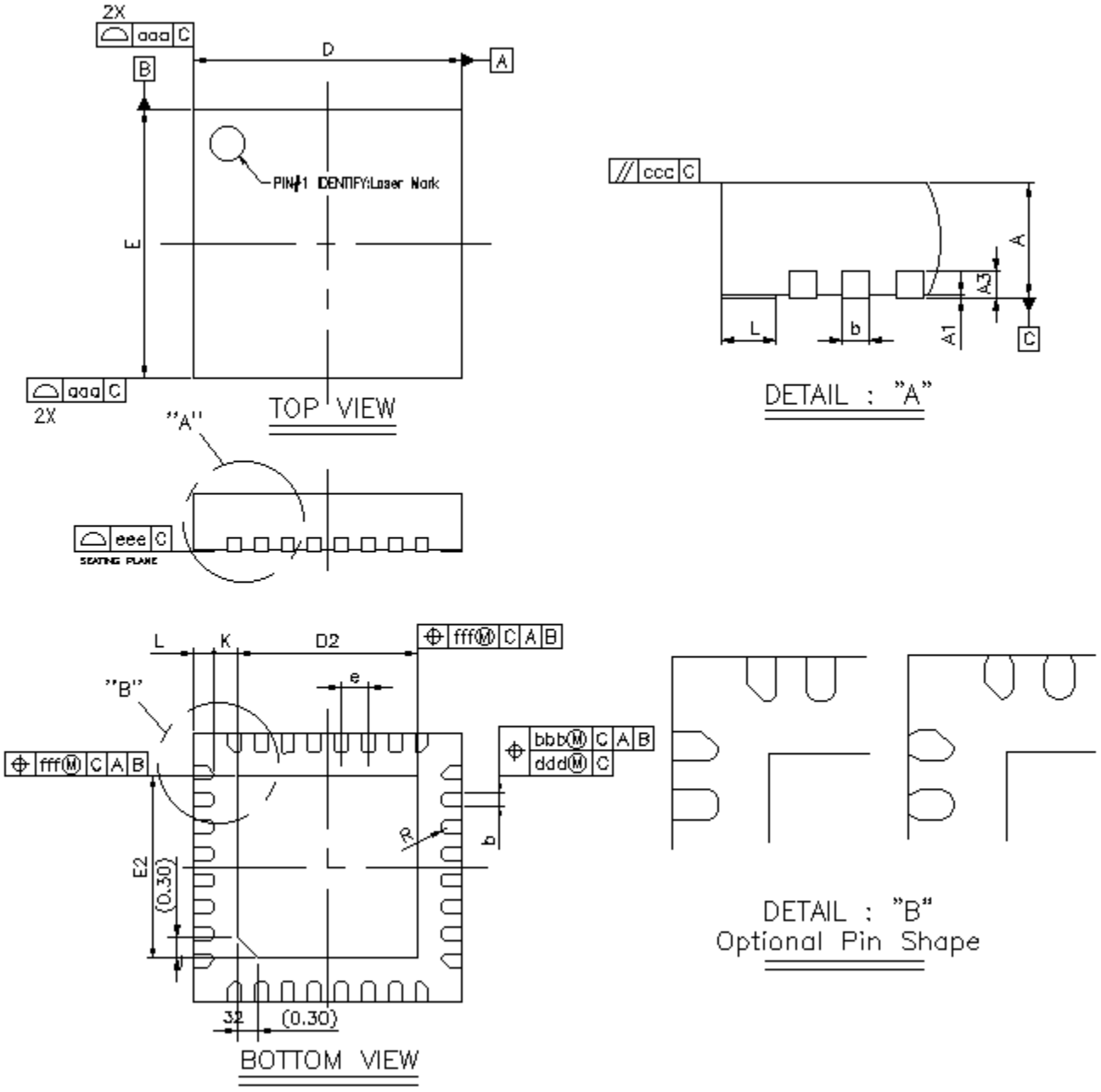

Figure 7.1. QFN32 Package Drawing

Table 7.1. QFN32 Package Dimensions

Dimension	Min	Typ	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A3		0.20 REF	
b	0.15	0.20	0.25
D	3.90	4.00	4.10
E	3.90	4.00	4.10
D2	2.60	2.70	2.80
E2	2.60	2.70	2.80
e		0.40 BSC	
L	0.20	0.30	0.40
K	0.20	—	—
R	0.075	—	0.125
aaa		0.10	
bbb		0.07	
ccc		0.10	
ddd		0.05	
eee		0.08	
fff		0.10	

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-220, Variation VKKD-4.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

7.2 QFN32 PCB Land Pattern

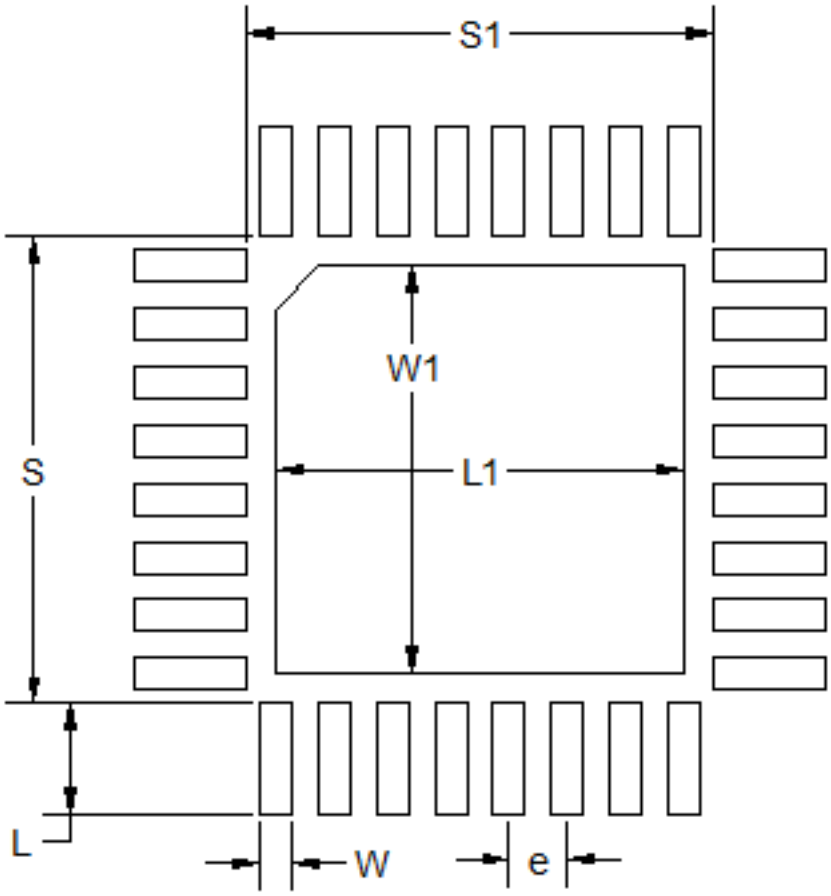

Figure 7.2. QFN32 PCB Land Pattern Drawing

Table 7.2. QFN32 PCB Land Pattern Dimensions

Dimension	Typ
L	0.76
W	0.22
e	0.40
S	3.21
S1	3.21
L1	2.80
W1	2.80

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.
4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
5. The stencil thickness should be 0.101 mm (4 mils).
6. The ratio of stencil aperture to land pad size can be 1:1 for all perimeter pads.
7. A 2x2 array of 1.10 mm x 1.10 mm openings on a 1.30 mm pitch can be used for the center ground pad.
8. A No-Clean, Type-3 solder paste is recommended.
9. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.
10. ***Above notes and stencil design are shared as recommendations only. A customer or user may find it necessary to use different parameters and fine tune their SMT process as required for their application and tooling.***

7.3 QFN32 Package Marking

Figure 7.3. QFN32 Package Marking

The package marking consists of:

- PPPPPPPP – The product option codes.
  - 1-7. The part number designation
  - 8. Flash (H = 512k | G = 256k | F = 128k | E = 64k)
- TTTTTT – A trace or manufacturing code. The first letter is the device revision.
- YY – The last 2 digits of the assembly year.
- WW – The 2-digit workweek when the device was assembled.
- # - The device revision.

8. QFN40 Package Specifications

8.1 QFN40 Package Dimensions

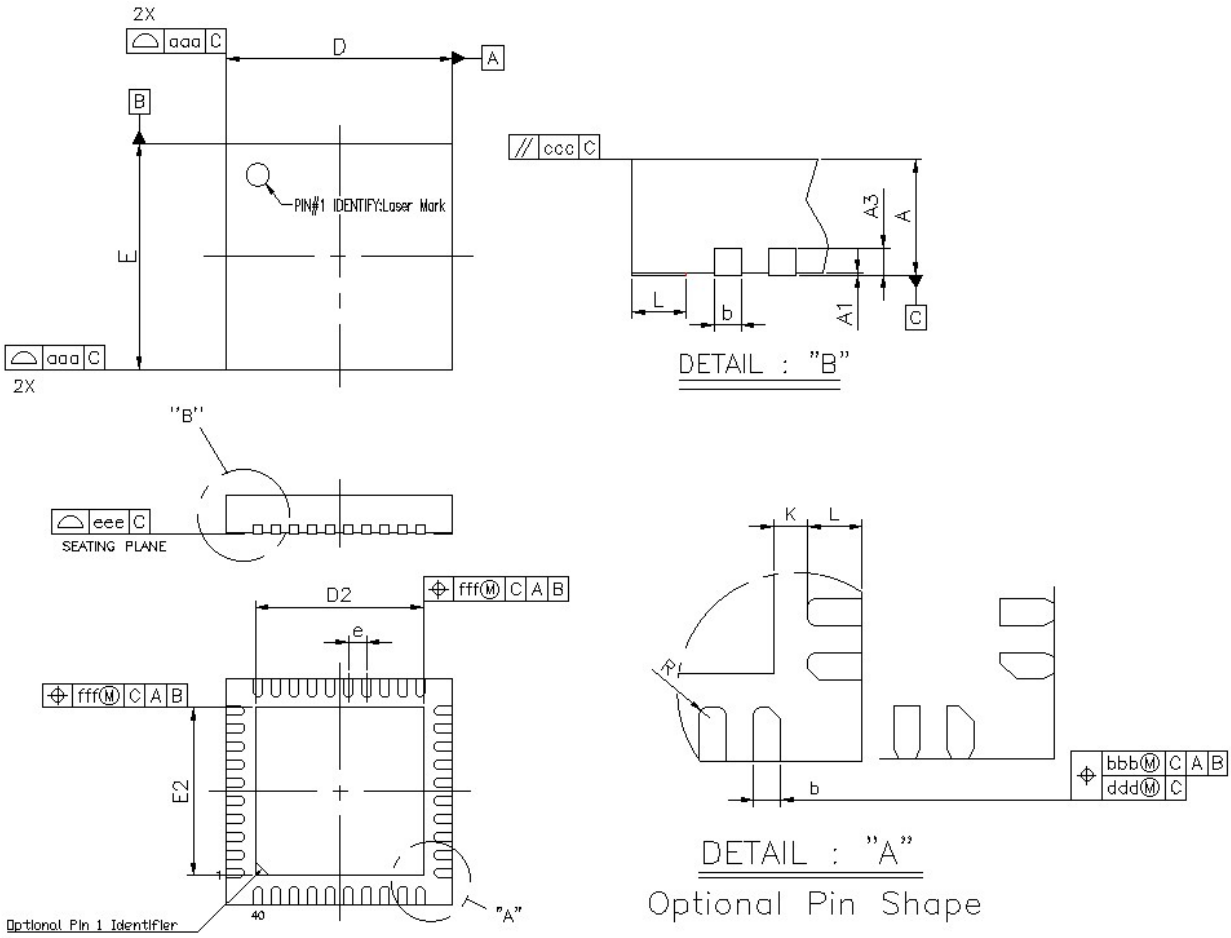

Figure 8.1. QFN40 Package Drawing

Table 8.1. QFN40 Package Dimensions

Dimension	Min	Typ	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A3		0.20 REF	
b	0.15	0.20	0.25
D	4.90	5.00	5.10
E	4.90	5.00	5.10
D2	3.55	3.70	3.85
E2	3.55	3.70	3.85
e		0.40 BSC	
L	0.30	0.40	0.50
K	0.20	—	—
R	0.075	—	—
aaa		0.10	
bbb		0.07	
ccc		0.10	
ddd		0.05	
eee		0.08	
fff		0.10	

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-220, Variation VKKD-4.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.
5. Package external pad (epad) may have pin one chamfer.

8.2 QFN40 PCB Land Pattern

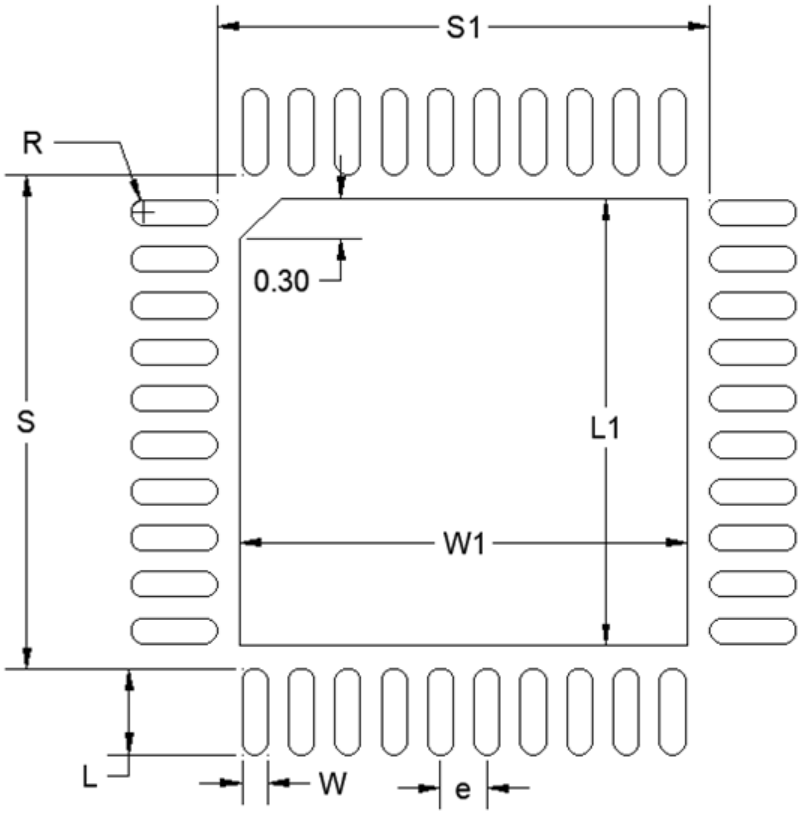

Figure 8.2. QFN40 PCB Land Pattern Drawing

Table 8.2. QFN40 PCB Land Pattern Dimensions

Dimension	Typ
S1	4.25
S	4.25
L1	3.85
W1	3.85
e	0.40
W	0.22
L	0.74
R	0.11

Dimension	Typ

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
4. The stencil thickness should be 0.101 mm (4 mils).
5. The ratio of stencil aperture to land pad size can be 1:1 for all perimeter pads.
6. A 3x3 array of 0.90 mm square openings on a 1.20 mm pitch can be used for the center ground pad.
7. A No-Clean, Type-3 solder paste is recommended.
8. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.
9. ***Above notes and stencil design are shared as recommendations only. A customer or user may find it necessary to use different parameters and fine tune their SMT process as required for their application and tooling.***

8.3 QFN40 Package Marking

Figure 8.3. QFN40 Package Marking

The package marking consists of:

- PPPPPPPPPP – The product option codes.
  - 1-9. The part number designation
  - 9. Flash (H = 512k | G = 256k | F = 128k | E = 64k)
  - 10. Temperature grade (I = -40 to 125 °C)
- TTTTTT – A trace or manufacturing code. The first letter is the device revision.
- YY – The last 2 digits of the assembly year.
- WW – The 2-digit workweek when the device was assembled.
- # - The device revision.

9. Revision History

Revision 1.3

June, 2024

- Updated and Figure 7.1 QFN32 Package Drawing on page 67 to include decoding of flash size and, when relevant, temperature range.
- Added 4.9 Boot Timing.
- Added Table 3.1 Secure Vault Features on page 11.
- Updated the test conditions for gain error in 4.12 Analog to Digital Converter (IADC).
- 4.12 Analog to Digital Converter (IADC):
  - Added input sampling capacitance for 3X gain.
  - Added input sampling frequency, and updated footnote.
  - Updated the test conditions for PSRR and gain error.
- Updated revision history v1.2 to remove the word draft.

Revision 1.2

March 2022

- Updated 8.3 QFN40 Package Marking.
- Updated Figure 7.1 QFN32 Package Drawing on page 67 with optional pin shapes to reflect multiple assembly sites.
- Added Figure 2.1 Ordering Code Key on page 4 and Table 2.1 Ordering Information on page 3.
- Updated max voltage on HFXO pins in Table 4.1 Absolute Maximum Ratings on page 18.
- Added CLKIN & DLLREFCLK max to Table 4.2 General Operating Conditions on page 19.
- Added startup time footnote in Table 4.11 High Frequency Crystal Oscillator on page 33 regarding programmable TIMEOUTSTEADY delay.
- Updated typical clock out current for HFRCODPLL in Table 4.13 High Frequency RC Oscillator (HFRCO) on page 35.
- Added ADC clock limitations for 2X, 3X and 4X gain in Table 4.18 Analog to Digital Converter (IADC) on page 40.
- Removed PB00 VERFN reference in Table 6.3 GPIO Alternate Function Table on page 62.
- Consolidated Table 6.3 GPIO Alternate Function Table on page 62 displaying support for dedicated functions across the different package options.
- Minor formatting and styling updates, including TOC locations and boilerplate information throughout document.

Revision 1.1

June 2021

- Updated lowest energy mode for I2C0, IADC0 and EUART0 to EM3 in 3.12 Configuration Summary.
- Added footnote for crystal load capacitance with Gain=2 test condition in 4.10.2 Low Frequency Crystal Oscillator.
- Added timing specification for RESETn low time in 4.11 GPIO Pins (3V GPIO pins).
- Added IADC 16 bit typical resolution and updated footnote in 4.12 Analog to Digital Converter (IADC).
- Corrected clock reference to PCLK in 4.16 USART SPI Main Timing and 4.17 USART SPI Secondary Timing.
- Corrected by removal IADC0.VREFN pinout from 6.3 Alternate Function Table; IADC0.VREFN connected internally to ground.
- Added documentation of chamfered pin 1 and oval land pattern in 8.1 QFN40 Package Dimensions.
- Replaced select terms with inclusive lexicon.
- Minor formatting and styling updates, including TOC locations and boilerplate information throughout document.

Revision 1.0

March, 2021

- Updated front page and feature list to reflect device offerings.
- Table 2.1 Ordering Information on page 3 updated to show all part numbers.
- 4.1 Electrical Characteristics updated throughout with full temperature range specifictions.
- Document updated throughout with additional information on higher-resolution ADC operation.
- 5.1 Power
  - Connection diagrams corrected to remove nonexistent supply pins, show crystals as optional.
  - Added text indicating IOVDD and AVDD are able to connect in other configurations.
  - Added third diagram with IOVDD and AVDD connected to DCDC output at DVDD.
- 32-pin QFN pinout information added.
- Package marking details updated.

Revision 0.1

April, 2020

Initial release.

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