

## FEATURES

- DC to 4.25 Gbps per port NRZ data rate**
- Adjustable receive equalization**
  - 3 dB, 6 dB, or 12 dB boost
- Compensates over 40 inches of FR4 at 4.25 Gbps**
- Adjustable transmit preemphasis/deemphasis**
  - Programmable boost and output level
- Compensates over 40 inches of FR4 at 4.25 Gbps**
- Low power**
  - 105 mW per channel at 2.5 V (400 mV p-p differential output level swing)
- 40 × 40, fully differential, nonblocking array**
  - Double rank connection programming with dual maps
- Low jitter, typically <25 ps**
- Flexible 2.5 V to 3.3 V supply range**
- DC- or ac-coupled differential PECL/CML inputs**
- Differential CML outputs**
- Per-lane polarity inversion for routing ease**
- 50 Ω on-chip I/O termination with disable feature**
- Supports 8b10b, scrambled or uncoded NRZ data**
- Serial (I<sup>2</sup>C slave or SPI) control interface**
- Parallel control interface**

## APPLICATIONS

- Digital video (HDMI, DVI, DisplayPort, 3G/HD/SD-SDI)**
- Fiber optic network switching**
- High speed serial backplane routing to OC-48 with FEC**
- XAUI, 4x Fibre Channel, Infiniband®, and GbE over backplane**
- Data storage networks**

## GENERAL DESCRIPTION

The ADN4605 is a 40 × 40 asynchronous, protocol agnostic, digital crosspoint switch, with 40 differential PECL/CML-compatible inputs and 40 differential programmable CML outputs.

The ADN4605 is optimized for NRZ signaling with data rates of up to 4.25 Gbps per port. Each port offers adjustable levels of input equalization, programmable output swing, and output preemphasis/deemphasis.

## FUNCTIONAL BLOCK DIAGRAM

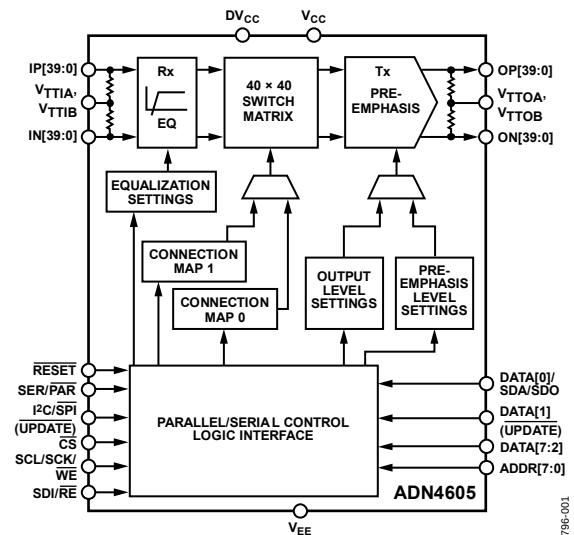


Figure 1.

The ADN4605 nonblocking switch core implements a 40 × 40 crossbar and supports independent channel switching through serial and parallel control interfaces. The ADN4605 has low latency and very low channel-to-channel skew.

An I<sup>2</sup>C, SPI, or parallel interface is used to communicate with the device for control of connectivity and other features.

The ADN4605 is assembled in a 35 mm × 35 mm, 352 BGA package and operates over a temperature range of −40°C to +85°C.

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## REVISION HISTORY

### 7/2019—Rev. A to Rev. B

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| Changes to Table 1 .....                                                       | 4  |
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### 11/2011—Rev. 0 to Rev. A

|                                                                   |    |
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| Removed Figure 55, Renumbered Sequentially .....                  | 54 |

### 6/2011—Revision 0: Initial Version

## SPECIFICATIONS

### ELECTRICAL SPECIFICATIONS

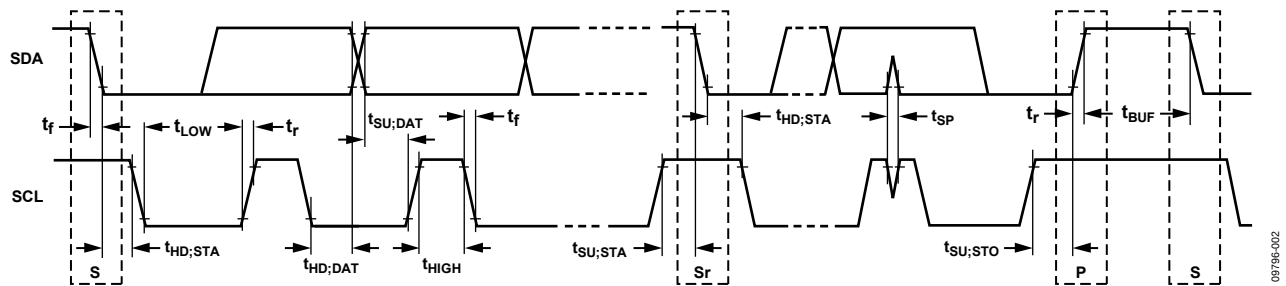
$V_{CC} = 2.5\text{ V}$ ,  $V_{TTk} = 2.5\text{ V}$ ,  $V_{TTOx} = 2.5\text{ V}$ ,  $DV_{CC} = 3.3\text{ V}$ ,  $V_{EE} = 0\text{ V}$ ,  $R_L = 50\ \Omega$ , output level (OLEV) = 4 (16 mA), preemphasis (PE) = 0 (0 dB), equalizer (EQ) = 1 (3 dB), data rate = 4.25 Gbps (PRBS7 data pattern), ac-coupled inputs and outputs, differential input swing = 800 mV p-p,  $T_A = 25^\circ\text{C}$ , unless otherwise noted.

Table 1.

| Parameter                                               | Conditions                                                                   | Min            | Typ            | Max            | Unit                    |
|---------------------------------------------------------|------------------------------------------------------------------------------|----------------|----------------|----------------|-------------------------|
| <b>DYNAMIC PERFORMANCE</b>                              |                                                                              |                |                |                |                         |
| Data Rate (DR) per Channel (NRZ)                        |                                                                              | dc             |                | 4.25           | Gbps                    |
| Deterministic Jitter                                    | Data rate $\leq 4.25$ Gbps, no channel                                       |                | 20             |                | ps p-p                  |
| Random Jitter                                           | RMS, no channel                                                              |                | 0.8            |                | ps rms                  |
| Residual Deterministic Jitter with Receive Equalization | Data rate = 4.25 Gbps, 20 in. FR4, EQ boost = 12 dB                          |                | 14             |                | ps p-p                  |
|                                                         | Data rate = 4.25 Gbps, 30 in. FR4, EQ boost = 12 dB                          |                | 15             |                | ps p-p                  |
|                                                         | Data rate = 4.25 Gbps, 40 in. FR4, EQ boost = 12 dB                          |                | 25             |                | ps p-p                  |
| Residual Deterministic Jitter with Transmit Preemphasis | Data rate = 4.25 Gbps, 20 in. FR4, PE boost = 5.6 dB                         |                | 22             |                | ps p-p                  |
|                                                         | Data rate = 4.25 Gbps, 30 in. FR4, PE boost = 6.8 dB                         |                | 28             |                | ps p-p                  |
|                                                         | Data rate = 4.25 Gbps, 40 in. FR4, PE boost = 9.5 dB                         |                | 32             |                | ps p-p                  |
| Propagation Delay                                       | Input to output                                                              |                | 920            |                | ps                      |
| Channel-to-Channel Skew                                 | Earliest input/output lane to latest input/output lane                       |                | 200            |                | ps                      |
| Switching Time                                          | Update logic switching to 50% output data                                    |                | 20             |                | ns                      |
| Output Rise/Fall Time                                   | 20% to 80%                                                                   |                | 108            |                | ps                      |
| <b>INPUT CHARACTERISTICS</b>                            |                                                                              |                |                |                |                         |
| Minimum Differential Input Voltage Swing <sup>1</sup>   | $V_{ICM} = V_{CC} - 0.6\text{ V}$                                            |                | 50             |                | mV p-p diff             |
| Maximum Differential Input Voltage Swing <sup>1</sup>   | $V_{ICM} = V_{CC} - 0.6\text{ V}$                                            |                | 2000           |                | mV p-p diff             |
| Input Voltage Range                                     | Single-ended absolute voltage level, $V_L$                                   | $V_{EE} + 1.0$ |                |                | V                       |
|                                                         | Single-ended absolute voltage level, $V_H$                                   |                |                | $V_{CC} + 0.3$ | V                       |
| <b>OUTPUT CHARACTERISTICS</b>                           |                                                                              |                |                |                |                         |
| Output Voltage Swing                                    | Differential, PE boost = 0 dB, default output level, at dc                   | 670            | 800            | 875            | mV p-p diff             |
| Output Voltage Range                                    | Single-ended absolute voltage level, $V_L$                                   |                | $V_{CC} - 1.4$ |                | V                       |
|                                                         | Single-ended absolute voltage level, $V_H$                                   |                | $V_{CC} + 0.3$ |                | V                       |
| Per-Port Output Current                                 | PE boost = 0 dB, default output level                                        |                | 16             |                | mA                      |
|                                                         | PE boost = 6 dB, default output level                                        |                | 32             |                | mA                      |
| <b>TERMINATION CHARACTERISTICS</b>                      |                                                                              |                |                |                |                         |
| Resistance                                              | Differential, $V_{CC} = V_{MIN}$ to $V_{MAX}$ , $T_A = T_{MIN}$ to $T_{MAX}$ | 88             | 100            | 114            | $\Omega$                |
| Temperature Coefficient                                 |                                                                              |                | 0.015          |                | $\Omega/^\circ\text{C}$ |
| <b>POWER SUPPLY</b>                                     |                                                                              |                |                |                |                         |
| <b>Operating Range</b>                                  |                                                                              |                |                |                |                         |
| $V_{CC}$                                                | $V_{EE} = 0\text{ V}$                                                        | 2.25           | 2.5            | 3.6            | V                       |
| $DV_{CC}$                                               | $V_{EE} = 0\text{ V}$                                                        | 3.0            | 3.3            | 3.6            | V                       |
| $V_{TTIA}$ , $V_{TTIB}$                                 | $V_{EE} = 0\text{ V}$                                                        |                | 2.5            | $V_{CC} + 0.3$ | V                       |
| $V_{TTOA}$ , $V_{TTOB}$                                 | $V_{EE} = 0\text{ V}$                                                        |                | 2.5            | $V_{CC} + 0.3$ | V                       |
| <b>Supply Current</b>                                   |                                                                              |                |                |                |                         |
| $I_{CC}$                                                | Inputs/outputs disabled (reset condition)                                    |                | 55             | 64             | mA                      |
| $I_{DVCC}$                                              |                                                                              |                | 0.3            | 1.1            | mA                      |
| $I_{TTIA} + I_{TTIB}$                                   | Inputs floating                                                              |                | 0              | 1.5            | mA                      |
| $I_{TTOA} + I_{TTOB}$                                   | Outputs floating                                                             |                | 0              | 1.5            | mA                      |

| Parameter                                 | Conditions                                                                                                                                | Min                   | Typ  | Max                   | Unit |
|-------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------|-----------------------|------|-----------------------|------|
| Supply Current                            | All outputs enabled, ac-coupled I/O,<br>200 mV I/O swings (400 mV p-p differential),<br>PE boost = 0 dB, 50 $\Omega$ far-end terminations |                       |      |                       |      |
| $I_{CC}$                                  |                                                                                                                                           |                       | 1320 | 1410                  | mA   |
| $I_{DVCC}$                                |                                                                                                                                           |                       | 0.3  | 1.1                   | mA   |
| $I_{TTIA} + I_{TTIB}$                     |                                                                                                                                           |                       | 11   | 15                    | mA   |
| $I_{TTOA} + I_{TTOB}$                     |                                                                                                                                           |                       | 335  | 360                   | mA   |
| Supply Current                            | All outputs enabled, ac-coupled I/O,<br>400 mV I/O swings (800 mV p-p differential),<br>PE boost = 0 dB, 50 $\Omega$ far-end terminations |                       |      |                       |      |
| $I_{CC}$                                  |                                                                                                                                           |                       | 1370 | 1460                  | mA   |
| $I_{DVCC}$                                |                                                                                                                                           |                       | 0.3  | 1.1                   | mA   |
| $I_{TTIA} + I_{TTIB}$                     |                                                                                                                                           |                       | 11   | 15                    | mA   |
| $I_{TTOA} + I_{TTOB}$                     |                                                                                                                                           |                       | 665  | 715                   | mA   |
| Supply Current                            | All outputs enabled, ac-coupled I/O,<br>400 mV I/O swings (800 mV p-p differential),<br>PE boost = 6 dB, 50 $\Omega$ far-end terminations |                       |      |                       |      |
| $I_{CC}$                                  |                                                                                                                                           |                       | 1850 | 1960                  | mA   |
| $I_{DVCC}$                                |                                                                                                                                           |                       | 0.3  | 1.1                   | mA   |
| $I_{TTIA} + I_{TTIB}$                     |                                                                                                                                           |                       | 11   | 15                    | mA   |
| $I_{TTOA} + I_{TTOB}$                     |                                                                                                                                           |                       | 1340 | 1380                  | mA   |
| LOGIC CHARACTERISTICS                     |                                                                                                                                           |                       |      |                       |      |
| Input High Voltage Threshold ( $V_{IH}$ ) | $DV_{CC} = 3.3\text{ V}$                                                                                                                  | $0.7 \times DV_{CC}$  |      |                       | V    |
| Input Low Voltage Threshold ( $V_{IL}$ )  | $DV_{CC} = 3.3\text{ V}$                                                                                                                  |                       |      | $0.25 \times DV_{CC}$ | V    |
| Output High Voltage ( $V_{OH}$ )          | $I_{OH} = -3\text{ mA}$ (I <sup>2</sup> C/SPI mode only)                                                                                  | $0.75 \times DV_{CC}$ |      | $DV_{CC}$             | V    |
| Output Low Voltage ( $V_{OL}$ )           | $I_{OL} = +3\text{ mA}$                                                                                                                   | $V_{EE}$              |      | 0.4                   | V    |

<sup>1</sup> $V_{ICM}$  is the input common-mode voltage.

I<sup>2</sup>C TIMING SPECIFICATIONSFigure 2. I<sup>2</sup>C Timing DiagramTable 2. I<sup>2</sup>C Timing Specifications

| Parameter                                                    | Symbol       | Min  | Max  | Unit    |
|--------------------------------------------------------------|--------------|------|------|---------|
| SCL Clock Frequency                                          | $f_{SCL}$    | 0    | 500+ | kHz     |
| Hold Time for a Start Condition                              | $t_{HD;STA}$ | 0.5  |      | $\mu$ s |
| Setup Time for a Repeated Start Condition                    | $t_{SU;STA}$ | 0.5  |      | $\mu$ s |
| Low Period of the SCL Clock                                  | $t_{LOW}$    |      | 1.4  | $\mu$ s |
| High Period of the SCL Clock                                 | $t_{HIGH}$   | 0.6  |      | $\mu$ s |
| Data Hold Time                                               | $t_{HD;DAT}$ | 0.02 |      | $\mu$ s |
| Data Setup Time                                              | $t_{SU;DAT}$ | 0.02 |      | $\mu$ s |
| Rise Time for Both SDA and SCL                               | $t_r$        | 1    | 300  | ns      |
| Fall Time for Both SDA and SCL                               | $t_f$        | 1    | 300  | ns      |
| Setup Time for Stop Condition                                | $t_{SU;STO}$ | 0.5  |      | $\mu$ s |
| Bus Free Time Between a Stop Condition and a Start Condition | $t_{BUF}$    | 1    |      | ns      |
| Bus Idle Time After a Reset                                  |              | 20   |      | ns      |
| Reset Pulse Width                                            |              | 20   |      | ns      |

## SPI TIMING SPECIFICATIONS

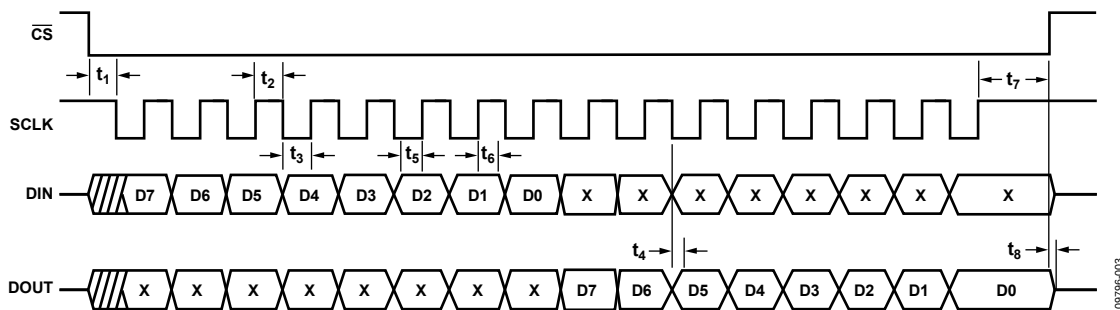


Figure 3. SPI Timing Diagram

Table 3. SPI Timing Specifications

| Parameter                                 | Symbol    | Min | Max | Unit |
|-------------------------------------------|-----------|-----|-----|------|
| SCK Clock Frequency                       | $f_{SCK}$ |     | 10  | MHz  |
| $\overline{CS}$ to SCLK Setup Time        | $t_1$     | 0   |     | ns   |
| SCLK High Pulse Width                     | $t_2$     | 30  |     | ns   |
| SCLK Low Pulse Width                      | $t_3$     | 30  |     | ns   |
| Data Access Time After SCLK Falling Edge  | $t_4$     |     | 45  | ns   |
| Data Setup Time Prior to SCLK Rising Edge | $t_5$     | 10  |     | ns   |
| Data Hold Time After SCLK Rising Edge     | $t_6$     | 30  |     | ns   |
| $\overline{CS}$ to SCLK Hold Time         | $t_7$     | 0   |     | ns   |
| $\overline{CS}$ to SDO High Impedance     | $t_8$     |     | 45  | ns   |
| Reset Pulse Width                         |           | 20  |     | ns   |

## PARALLEL MODE SPECIFICATIONS

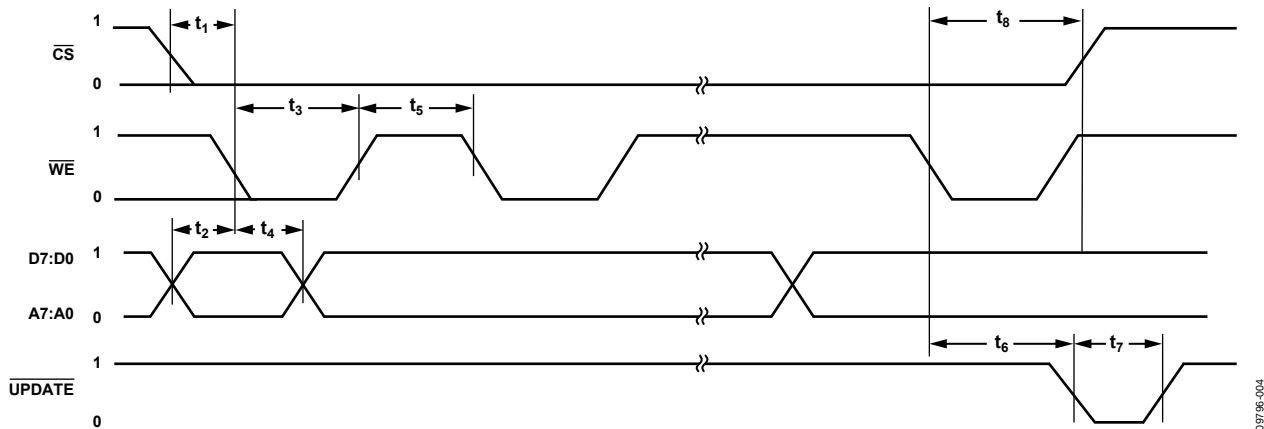


Figure 4. Parallel Mode Write Cycle

Table 4. Parallel Mode Write Cycle Timing Specifications

| Parameter                                    | Symbol | Min | Limit<br>Typ | Max | Unit |
|----------------------------------------------|--------|-----|--------------|-----|------|
| Chip Select Setup Time                       | $t_1$  | 0   |              |     | ns   |
| Parallel Data Setup Time                     | $t_2$  | 0   |              |     | ns   |
| $\overline{WE}$ Pulse Width                  | $t_3$  | 30  | 50           |     | ns   |
| Parallel Data Hold Time                      | $t_4$  | 25  |              |     | ns   |
| $\overline{WE}$ Pulse Separation             | $t_5$  |     | 25           |     | ns   |
| $\overline{WE}$ to $\overline{UPDATE}$ Delay | $t_6$  |     | 40           |     | ns   |
| $\overline{UPDATE}$ Pulse Width              | $t_7$  | 30  |              |     | ns   |
| Chip Select Hold Time                        | $t_8$  | 0   |              |     | ns   |
| Reset Pulse Width                            |        | 20  |              |     | ns   |

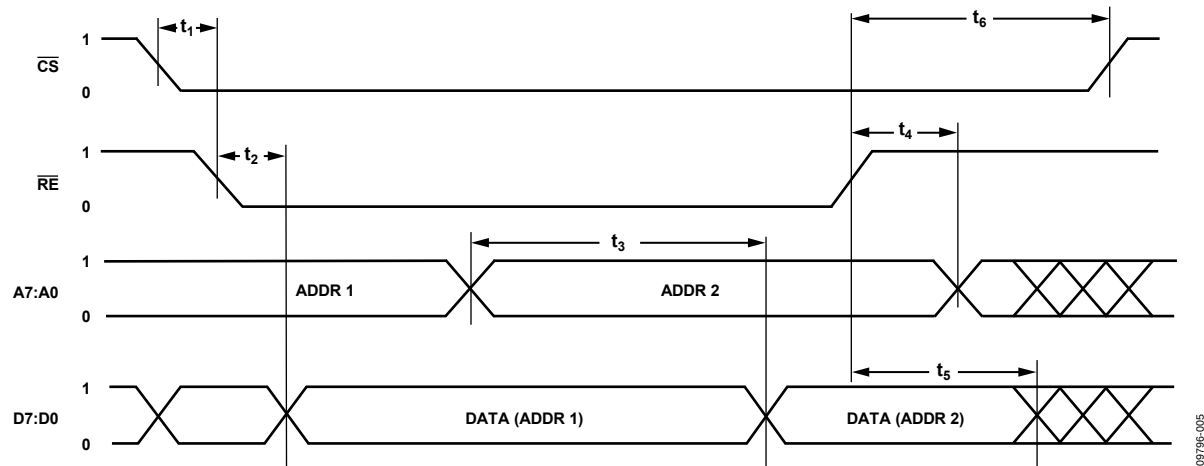


Figure 5. Parallel Mode Read Cycle

Table 5. Parallel Mode Read Cycle Timing Specifications

| Parameter                                    | Symbol | Min | Limit<br>Typ | Max | Unit |
|----------------------------------------------|--------|-----|--------------|-----|------|
| Chip Select Setup Time                       | $t_1$  | 0   |              |     | ns   |
| Parallel $\overline{RE}$ Setup to Valid Time | $t_2$  | 10  |              |     | ns   |
| Data Access Time                             | $t_3$  | 25  | 50           |     | ns   |
| Address to $\overline{RE}$ Hold Time         | $t_4$  | 25  |              |     | ns   |
| Data to $\overline{RE}$ Hold Time            | $t_5$  | 25  |              |     | ns   |
| Chip Select Hold Time                        | $t_6$  | 5   |              |     | ns   |

## ABSOLUTE MAXIMUM RATINGS

Table 6.

| Parameter                               | Rating                                         |
|-----------------------------------------|------------------------------------------------|
| $V_{CC}$ to $V_{EE}$                    | 3.7 V                                          |
| $DV_{CC}$ to $V_{EE}$                   | 3.7 V                                          |
| $V_{TTIA}$ , $V_{TTIB}$                 | $V_{CC} + 0.6$ V                               |
| $V_{TTOA}$ , $V_{TTOB}$                 | $V_{CC} + 0.6$ V                               |
| Internal Power Dissipation <sup>1</sup> | 11.5 W                                         |
| Differential Input Voltage              | 2.0 V                                          |
| Logic Input Voltage                     | $V_{EE} - 0.3$ V < $V_{IN}$ < $V_{CC} + 0.6$ V |
| Storage Temperature Range               | -65°C to +125°C                                |
| Junction Temperature                    | 125°C                                          |

<sup>1</sup> The internal power dissipation is for the device in free air.  $T_A = 25^\circ\text{C}$  and  $\theta_{JA} = 8.5^\circ\text{C/W}$  in still air.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

## THERMAL RESISTANCE

Thermal resistance values specified in Table 7 are simulated based on JEDEC specs (unless specified otherwise) and must be used in compliance with JESD51-12. Using enhanced heat removal (printed circuit board (PCB), heat sink, or airflow) technique improves thermal resistance values.

Table 7. Thermal Resistance Values

| Package Type | $\theta_{JA}$<br>(°C/W) | $\theta_{JC\_TOP}$ <sup>1</sup><br>(°C/W) | $\Psi_{JT}$<br>(°C/W) | $\Psi_{JB}$<br>(°C/W) |
|--------------|-------------------------|-------------------------------------------|-----------------------|-----------------------|
| BP-352-2     | 8.5                     | 0.3                                       | 0.2                   | 2.4                   |

<sup>1</sup> For the  $\theta_{JC\_TOP}$  test, 100  $\mu\text{m}$  thermal insulation material (TIM) is used. The TIM is assumed to have 3.6 W/m K.

## ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

|    | 1               | 2               | 3                 | 4                        | 5               | 6               | 7                 | 8                 | 9                 | 10                | 11              | 12              | 13                | 14                | 15                | 16              | 17              | 18                | 19                | 20                | 21                | 22              | 23               | 24                | 25              | 26              |    |
|----|-----------------|-----------------|-------------------|--------------------------|-----------------|-----------------|-------------------|-------------------|-------------------|-------------------|-----------------|-----------------|-------------------|-------------------|-------------------|-----------------|-----------------|-------------------|-------------------|-------------------|-------------------|-----------------|------------------|-------------------|-----------------|-----------------|----|
| A  | V <sub>EE</sub> | V <sub>EE</sub> | V <sub>EE</sub>   | ON39                     | OP39            | ON37            | OP37              | ON35              | OP35              | ON33              | OP33            | ON31            | OP31              | ON29              | OP29              | ON27            | OP27            | ON25              | OP25              | ON23              | OP23              | ON21            | OP21             | V <sub>EE</sub>   | V <sub>EE</sub> | V <sub>EE</sub> | A  |
| B  | V <sub>EE</sub> | V <sub>EE</sub> | V <sub>EE</sub>   | V <sub>EE</sub>          | ON38            | OP38            | ON36              | OP36              | ON34              | OP34              | ON32            | OP32            | ON30              | OP30              | ON28              | OP28            | ON26            | OP26              | ON24              | OP24              | ON22              | OP22            | ON20             | OP20              | V <sub>EE</sub> | V <sub>EE</sub> | B  |
| C  | V <sub>EE</sub> | IP0             | V <sub>EE</sub>   | V <sub>CC</sub>          | V <sub>CC</sub> | V <sub>CC</sub> | V <sub>TT0B</sub> | V <sub>TT0B</sub> | V <sub>TT0B</sub> | V <sub>TT0B</sub> | V <sub>CC</sub> | V <sub>CC</sub> | V <sub>TT0B</sub> | V <sub>TT0B</sub> | V <sub>TT0B</sub> | V <sub>CC</sub> | V <sub>CC</sub> | V <sub>TT0B</sub> | V <sub>TT0B</sub> | V <sub>TT0B</sub> | V <sub>TT0B</sub> | V <sub>CC</sub> | V <sub>CC</sub>  | DV <sub>CC</sub>  | V <sub>EE</sub> | V <sub>EE</sub> | C  |
| D  | IP1             | IN0             | V <sub>CC</sub>   | DV <sub>CC</sub>         | V <sub>CC</sub> | V <sub>CC</sub> | V <sub>EE</sub>   | V <sub>EE</sub>   | V <sub>EE</sub>   | V <sub>EE</sub>   | V <sub>CC</sub> | V <sub>CC</sub> | V <sub>EE</sub>   | V <sub>EE</sub>   | V <sub>EE</sub>   | V <sub>CC</sub> | V <sub>CC</sub> | V <sub>EE</sub>   | V <sub>EE</sub>   | V <sub>EE</sub>   | V <sub>EE</sub>   | V <sub>CC</sub> | DV <sub>CC</sub> | V <sub>CC</sub>   | V <sub>EE</sub> | IN39            | D  |
| E  | IN1             | IP2             | V <sub>CC</sub>   | V <sub>EE</sub>          |                 |                 |                   |                   |                   |                   |                 |                 |                   |                   |                   |                 |                 |                   |                   |                   |                   |                 | V <sub>EE</sub>  | V <sub>CC</sub>   | IN38            | IP39            | E  |
| F  | IP3             | IN2             | V <sub>TTIA</sub> | V <sub>EE</sub>          |                 |                 |                   |                   |                   |                   |                 |                 |                   |                   |                   |                 |                 |                   |                   |                   |                   |                 | V <sub>EE</sub>  | V <sub>TTIB</sub> | IP38            | IN37            | F  |
| G  | IN3             | IP4             | V <sub>TTIA</sub> | V <sub>EE</sub>          |                 |                 |                   |                   |                   |                   |                 |                 |                   |                   |                   |                 |                 |                   |                   |                   |                   |                 | V <sub>EE</sub>  | V <sub>TTIB</sub> | IN36            | IP37            | G  |
| H  | IP5             | IN4             | V <sub>TTIA</sub> | V <sub>EE</sub>          |                 |                 |                   |                   |                   |                   |                 |                 |                   |                   |                   |                 |                 |                   |                   |                   |                   |                 | $\overline{WE}$  | V <sub>TTIB</sub> | IP36            | IN35            | H  |
| J  | IN5             | IP6             | V <sub>TTIA</sub> | I <sup>2</sup> C/<br>SPI |                 |                 |                   |                   |                   |                   |                 |                 |                   |                   |                   |                 |                 |                   |                   |                   |                   |                 | $\overline{RE}$  | V <sub>TTIB</sub> | IN34            | IP35            | J  |
| K  | IP7             | IN6             | V <sub>CC</sub>   | SER/<br>PAR              |                 |                 |                   |                   |                   |                   |                 |                 |                   |                   |                   |                 |                 |                   |                   |                   |                   |                 | CS               | V <sub>CC</sub>   | IP34            | IN33            | K  |
| L  | IN7             | IP8             | V <sub>CC</sub>   | RESET                    |                 |                 |                   |                   |                   |                   |                 |                 |                   |                   |                   |                 |                 |                   |                   |                   |                   |                 | DATA0            | V <sub>CC</sub>   | IN32            | IP33            | L  |
| M  | IP9             | IN8             | V <sub>TTIA</sub> | ADDR0                    |                 |                 |                   |                   |                   |                   |                 |                 |                   |                   |                   |                 |                 |                   |                   |                   |                   |                 | DATA1            | V <sub>TTIB</sub> | IP32            | IN31            | M  |
| N  | IN9             | IP10            | V <sub>TTIA</sub> | ADDR1                    |                 |                 |                   |                   |                   |                   |                 |                 |                   |                   |                   |                 |                 |                   |                   |                   |                   |                 | DATA2            | V <sub>TTIB</sub> | IN30            | IP31            | N  |
| P  | IP11            | IN10            | V <sub>TTIA</sub> | ADDR2                    |                 |                 |                   |                   |                   |                   |                 |                 |                   |                   |                   |                 |                 |                   |                   |                   |                   |                 | DATA3            | V <sub>TTIB</sub> | IP30            | IN29            | P  |
| R  | IN11            | IP12            | V <sub>CC</sub>   | ADDR3                    |                 |                 |                   |                   |                   |                   |                 |                 |                   |                   |                   |                 |                 |                   |                   |                   |                   |                 | DATA4            | V <sub>CC</sub>   | IN28            | IP29            | R  |
| T  | IP13            | IN12            | V <sub>CC</sub>   | ADDR4                    |                 |                 |                   |                   |                   |                   |                 |                 |                   |                   |                   |                 |                 |                   |                   |                   |                   |                 | DATA5            | V <sub>CC</sub>   | IP28            | IN27            | T  |
| U  | IN13            | IP14            | V <sub>TTIA</sub> | ADDR5                    |                 |                 |                   |                   |                   |                   |                 |                 |                   |                   |                   |                 |                 |                   |                   |                   |                   |                 | DATA6            | V <sub>TTIB</sub> | IN26            | IP27            | U  |
| V  | IP15            | IN14            | V <sub>TTIA</sub> | ADDR6                    |                 |                 |                   |                   |                   |                   |                 |                 |                   |                   |                   |                 |                 |                   |                   |                   |                   |                 | DATA7            | V <sub>TTIB</sub> | IP26            | IN25            | V  |
| W  | IN15            | IP16            | V <sub>TTIA</sub> | ADDR7                    |                 |                 |                   |                   |                   |                   |                 |                 |                   |                   |                   |                 |                 |                   |                   |                   |                   |                 | V <sub>EE</sub>  | V <sub>TTIB</sub> | IN24            | IP25            | W  |
| Y  | IP17            | IN16            | V <sub>TTIA</sub> | V <sub>EE</sub>          |                 |                 |                   |                   |                   |                   |                 |                 |                   |                   |                   |                 |                 |                   |                   |                   |                   |                 | V <sub>EE</sub>  | V <sub>TTIB</sub> | IP24            | IN23            | Y  |
| AA | IN17            | IP18            | V <sub>CC</sub>   | V <sub>EE</sub>          |                 |                 |                   |                   |                   |                   |                 |                 |                   |                   |                   |                 |                 |                   |                   |                   |                   |                 | V <sub>EE</sub>  | V <sub>CC</sub>   | IN22            | IP23            | AA |
| AB | IP19            | IN18            | V <sub>CC</sub>   | V <sub>EE</sub>          |                 |                 |                   |                   |                   |                   |                 |                 |                   |                   |                   |                 |                 |                   |                   |                   |                   |                 | V <sub>EE</sub>  | V <sub>CC</sub>   | IP22            | IN21            | AB |
| AC | IN19            | V <sub>EE</sub> | V <sub>CC</sub>   | DV <sub>CC</sub>         | V <sub>CC</sub> | V <sub>CC</sub> | V <sub>EE</sub>   | V <sub>EE</sub>   | V <sub>EE</sub>   | V <sub>EE</sub>   | V <sub>CC</sub> | V <sub>CC</sub> | V <sub>EE</sub>   | V <sub>EE</sub>   | V <sub>EE</sub>   | V <sub>CC</sub> | V <sub>CC</sub> | V <sub>EE</sub>   | V <sub>EE</sub>   | V <sub>EE</sub>   | V <sub>EE</sub>   | V <sub>CC</sub> | DV <sub>CC</sub> | V <sub>CC</sub>   | IN20            | IP21            | AC |
| AD | V <sub>EE</sub> | V <sub>EE</sub> | V <sub>EE</sub>   | V <sub>CC</sub>          | V <sub>CC</sub> | V <sub>CC</sub> | V <sub>TT0A</sub> | V <sub>TT0A</sub> | V <sub>TT0A</sub> | V <sub>TT0A</sub> | V <sub>CC</sub> | V <sub>CC</sub> | V <sub>TT0A</sub> | V <sub>TT0A</sub> | V <sub>TT0A</sub> | V <sub>CC</sub> | V <sub>CC</sub> | V <sub>TT0A</sub> | V <sub>TT0A</sub> | V <sub>TT0A</sub> | V <sub>TT0A</sub> | V <sub>CC</sub> | V <sub>CC</sub>  | V <sub>EE</sub>   | IP20            | V <sub>EE</sub> | AD |
| AE | V <sub>EE</sub> | V <sub>EE</sub> | OP0               | ON0                      | OP2             | ON2             | OP4               | ON4               | OP6               | ON6               | OP8             | ON8             | OP10              | ON10              | OP12              | ON12            | OP14            | ON14              | OP16              | ON16              | OP18              | ON18            | V <sub>EE</sub>  | V <sub>EE</sub>   | V <sub>EE</sub> | V <sub>EE</sub> | AE |
| AF | V <sub>EE</sub> | V <sub>EE</sub> | V <sub>EE</sub>   | OP1                      | ON1             | OP3             | ON3               | OP5               | ON5               | OP7               | ON7             | OP9             | ON9               | OP11              | ON11              | OP13            | ON13            | OP15              | ON15              | OP17              | ON17              | OP19            | ON19             | V <sub>EE</sub>   | V <sub>EE</sub> | V <sub>EE</sub> | AF |
|    | 1               | 2               | 3                 | 4                        | 5               | 6               | 7                 | 8                 | 9                 | 10                | 11              | 12              | 13                | 14                | 15                | 16              | 17              | 18                | 19                | 20                | 21                | 22              | 23               | 24                | 25              | 26              |    |

ADN4605  
Top View

09796-006

Figure 6. Pin Configuration

Table 8. Pin Function Descriptions

| Pin No. | Mnemonic        | Type   | Description                   |
|---------|-----------------|--------|-------------------------------|
| A1      | V <sub>EE</sub> | Power  | Negative Supply.              |
| A2      | V <sub>EE</sub> | Power  | Negative Supply.              |
| A3      | V <sub>EE</sub> | Power  | Negative Supply.              |
| A4      | ON39            | Output | High Speed Output Complement. |
| A5      | OP39            | Output | High Speed Output.            |
| A6      | ON37            | Output | High Speed Output Complement. |
| A7      | OP37            | Output | High Speed Output.            |
| A8      | ON35            | Output | High Speed Output Complement. |
| A9      | OP35            | Output | High Speed Output.            |
| A10     | ON33            | Output | High Speed Output Complement. |
| A11     | OP33            | Output | High Speed Output.            |
| A12     | ON31            | Output | High Speed Output Complement. |
| A13     | OP31            | Output | High Speed Output.            |
| A14     | ON29            | Output | High Speed Output Complement. |
| A15     | OP29            | Output | High Speed Output.            |
| A16     | ON27            | Output | High Speed Output Complement. |
| A17     | OP27            | Output | High Speed Output.            |
| A18     | ON25            | Output | High Speed Output Complement. |
| A19     | OP25            | Output | High Speed Output.            |
| A20     | ON23            | Output | High Speed Output Complement. |
| A21     | OP23            | Output | High Speed Output.            |
| A22     | ON21            | Output | High Speed Output Complement. |
| A23     | OP21            | Output | High Speed Output.            |
| A24     | V <sub>EE</sub> | Power  | Negative Supply.              |
| A25     | V <sub>EE</sub> | Power  | Negative Supply.              |
| A26     | V <sub>EE</sub> | Power  | Negative Supply.              |
| B1      | V <sub>EE</sub> | Power  | Negative Supply.              |
| B2      | V <sub>EE</sub> | Power  | Negative Supply.              |
| B3      | V <sub>EE</sub> | Power  | Negative Supply.              |
| B4      | V <sub>EE</sub> | Power  | Negative Supply.              |
| B5      | ON38            | Output | High Speed Output Complement. |
| B6      | OP38            | Output | High Speed Output.            |
| B7      | ON36            | Output | High Speed Output Complement. |
| B8      | OP36            | Output | High Speed Output.            |
| B9      | ON34            | Output | High Speed Output Complement. |
| B10     | OP34            | Output | High Speed Output.            |
| B11     | ON32            | Output | High Speed Output Complement. |
| B12     | OP32            | Output | High Speed Output.            |
| B13     | ON30            | Output | High Speed Output Complement. |
| B14     | OP30            | Output | High Speed Output.            |
| B15     | ON28            | Output | High Speed Output Complement. |
| B16     | OP28            | Output | High Speed Output.            |
| B17     | ON26            | Output | High Speed Output Complement. |
| B18     | OP26            | Output | High Speed Output.            |
| B19     | ON24            | Output | High Speed Output Complement. |
| B20     | OP24            | Output | High Speed Output.            |
| B21     | ON22            | Output | High Speed Output Complement. |
| B22     | OP22            | Output | High Speed Output.            |

| Pin No. | Mnemonic          | Type   | Description                                                                                                |
|---------|-------------------|--------|------------------------------------------------------------------------------------------------------------|
| B23     | ON20              | Output | High Speed Output Complement.                                                                              |
| B24     | OP20              | Output | High Speed Output.                                                                                         |
| B25     | V <sub>EE</sub>   | Power  | Negative Supply.                                                                                           |
| B26     | V <sub>EE</sub>   | Power  | Negative Supply.                                                                                           |
| C1      | V <sub>EE</sub>   | Power  | Negative Supply.                                                                                           |
| C2      | IP0               | Input  | High Speed Input.                                                                                          |
| C3      | V <sub>EE</sub>   | Power  | Negative Supply.                                                                                           |
| C4      | V <sub>CC</sub>   | Power  | Positive Supply.                                                                                           |
| C5      | V <sub>CC</sub>   | Power  | Positive Supply.                                                                                           |
| C6      | V <sub>CC</sub>   | Power  | Positive Supply.                                                                                           |
| C7      | V <sub>TTOB</sub> | Power  | Output Termination Supply (B). The V <sub>TTOB</sub> pins are normally tied to the V <sub>TTOA</sub> pins. |
| C8      | V <sub>TTOB</sub> | Power  | Output Termination Supply (B). The V <sub>TTOB</sub> pins are normally tied to the V <sub>TTOA</sub> pins. |
| C9      | V <sub>TTOB</sub> | Power  | Output Termination Supply (B). The V <sub>TTOB</sub> pins are normally tied to the V <sub>TTOA</sub> pins. |
| C10     | V <sub>TTOB</sub> | Power  | Output Termination Supply (B). The V <sub>TTOB</sub> pins are normally tied to the V <sub>TTOA</sub> pins. |
| C11     | V <sub>CC</sub>   | Power  | Positive Supply.                                                                                           |
| C12     | V <sub>CC</sub>   | Power  | Positive Supply.                                                                                           |
| C13     | V <sub>TTOB</sub> | Power  | Output Termination Supply (B). The V <sub>TTOB</sub> pins are normally tied to the V <sub>TTOA</sub> pins. |
| C14     | V <sub>TTOB</sub> | Power  | Output Termination Supply (B). The V <sub>TTOB</sub> pins are normally tied to the V <sub>TTOA</sub> pins. |
| C15     | V <sub>TTOB</sub> | Power  | Output Termination Supply (B). The V <sub>TTOB</sub> pins are normally tied to the V <sub>TTOA</sub> pins. |
| C16     | V <sub>CC</sub>   | Power  | Positive Supply.                                                                                           |
| C17     | V <sub>CC</sub>   | Power  | Positive Supply.                                                                                           |
| C18     | V <sub>TTOB</sub> | Power  | Output Termination Supply (B). The V <sub>TTOB</sub> pins are normally tied to the V <sub>TTOA</sub> pins. |
| C19     | V <sub>TTOB</sub> | Power  | Output Termination Supply (B). The V <sub>TTOB</sub> pins are normally tied to the V <sub>TTOA</sub> pins. |
| C20     | V <sub>TTOB</sub> | Power  | Output Termination Supply (B). The V <sub>TTOB</sub> pins are normally tied to the V <sub>TTOA</sub> pins. |
| C21     | V <sub>TTOB</sub> | Power  | Output Termination Supply (B). The V <sub>TTOB</sub> pins are normally tied to the V <sub>TTOA</sub> pins. |
| C22     | V <sub>CC</sub>   | Power  | Positive Supply.                                                                                           |
| C23     | V <sub>CC</sub>   | Power  | Positive Supply.                                                                                           |
| C24     | DV <sub>CC</sub>  | Power  | Digital Positive Supply.                                                                                   |
| C25     | V <sub>EE</sub>   | Power  | Negative Supply.                                                                                           |
| C26     | V <sub>EE</sub>   | Power  | Negative Supply.                                                                                           |
| D1      | IP1               | Input  | High Speed Input.                                                                                          |
| D2      | IN0               | Input  | High Speed Input Complement.                                                                               |
| D3      | V <sub>CC</sub>   | Power  | Positive Supply.                                                                                           |
| D4      | DV <sub>CC</sub>  | Power  | Digital Positive Supply.                                                                                   |
| D5      | V <sub>CC</sub>   | Power  | Positive Supply.                                                                                           |
| D6      | V <sub>CC</sub>   | Power  | Positive Supply.                                                                                           |
| D7      | V <sub>EE</sub>   | Power  | Negative Supply.                                                                                           |
| D8      | V <sub>EE</sub>   | Power  | Negative Supply.                                                                                           |
| D9      | V <sub>EE</sub>   | Power  | Negative Supply.                                                                                           |
| D10     | V <sub>EE</sub>   | Power  | Negative Supply.                                                                                           |
| D11     | V <sub>CC</sub>   | Power  | Positive Supply.                                                                                           |
| D12     | V <sub>CC</sub>   | Power  | Positive Supply.                                                                                           |

| Pin No. | Mnemonic                | Type    | Description                                                                                                                                                                                         |
|---------|-------------------------|---------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| D13     | V <sub>EE</sub>         | Power   | Negative Supply.                                                                                                                                                                                    |
| D14     | V <sub>EE</sub>         | Power   | Negative Supply.                                                                                                                                                                                    |
| D15     | V <sub>EE</sub>         | Power   | Negative Supply.                                                                                                                                                                                    |
| D16     | V <sub>CC</sub>         | Power   | Positive Supply.                                                                                                                                                                                    |
| D17     | V <sub>CC</sub>         | Power   | Positive Supply.                                                                                                                                                                                    |
| D18     | V <sub>EE</sub>         | Power   | Negative Supply.                                                                                                                                                                                    |
| D19     | V <sub>EE</sub>         | Power   | Negative Supply.                                                                                                                                                                                    |
| D20     | V <sub>EE</sub>         | Power   | Negative Supply.                                                                                                                                                                                    |
| D21     | V <sub>EE</sub>         | Power   | Negative Supply.                                                                                                                                                                                    |
| D22     | V <sub>CC</sub>         | Power   | Positive Supply.                                                                                                                                                                                    |
| D23     | DV <sub>CC</sub>        | Power   | Digital Positive Supply.                                                                                                                                                                            |
| D24     | V <sub>CC</sub>         | Power   | Positive Supply.                                                                                                                                                                                    |
| D25     | V <sub>EE</sub>         | Power   | Negative Supply.                                                                                                                                                                                    |
| D26     | IN39                    | Input   | High Speed Input Complement.                                                                                                                                                                        |
| E1      | IN1                     | Input   | High Speed Input Complement.                                                                                                                                                                        |
| E2      | IP2                     | Input   | High Speed Input.                                                                                                                                                                                   |
| E3      | V <sub>CC</sub>         | Power   | Positive Supply.                                                                                                                                                                                    |
| E4      | V <sub>EE</sub>         | Power   | Negative Supply.                                                                                                                                                                                    |
| E23     | V <sub>EE</sub>         | Power   | Negative Supply.                                                                                                                                                                                    |
| E24     | V <sub>CC</sub>         | Power   | Positive Supply.                                                                                                                                                                                    |
| E25     | IN38                    | Input   | High Speed Input Complement.                                                                                                                                                                        |
| E26     | IP39                    | Input   | High Speed Input                                                                                                                                                                                    |
| F1      | IP3                     | Input   | High Speed Input                                                                                                                                                                                    |
| F2      | IN2                     | Input   | High Speed Input Complement.                                                                                                                                                                        |
| F3      | V <sub>TTIA</sub>       | Power   | Input Termination Supply (A). The V <sub>TTIA</sub> pins are normally tied to the V <sub>TTIB</sub> pins.                                                                                           |
| F4      | V <sub>EE</sub>         | Power   | Negative Supply.                                                                                                                                                                                    |
| F23     | V <sub>EE</sub>         | Power   | Negative Supply.                                                                                                                                                                                    |
| F24     | V <sub>TTIB</sub>       | Power   | Input Termination Supply (B). The V <sub>TTIB</sub> pins are normally tied to the V <sub>TTIA</sub> pins.                                                                                           |
| F25     | IP38                    | Input   | High Speed Input.                                                                                                                                                                                   |
| F26     | IN37                    | Input   | High Speed Input Complement.                                                                                                                                                                        |
| G1      | IN3                     | Input   | High Speed Input Complement.                                                                                                                                                                        |
| G2      | IP4                     | Input   | High Speed Input.                                                                                                                                                                                   |
| G3      | V <sub>TTIA</sub>       | Power   | Input Termination Supply (A). The V <sub>TTIA</sub> pins are normally tied to the V <sub>TTIB</sub> pins.                                                                                           |
| G4      | V <sub>EE</sub>         | Power   | Negative Supply.                                                                                                                                                                                    |
| G23     | V <sub>EE</sub>         | Power   | Negative Supply.                                                                                                                                                                                    |
| G24     | V <sub>TTIB</sub>       | Power   | Input Termination Supply (B). The V <sub>TTIB</sub> pins are normally tied to the V <sub>TTIA</sub> pins.                                                                                           |
| G25     | IN36                    | Input   | High Speed Input Complement.                                                                                                                                                                        |
| G26     | IP37                    | Input   | High Speed Input.                                                                                                                                                                                   |
| H1      | IP5                     | Input   | High Speed Input.                                                                                                                                                                                   |
| H2      | IN4                     | Input   | High Speed Input Complement.                                                                                                                                                                        |
| H3      | V <sub>TTIA</sub>       | Power   | Input Termination Supply (A). The V <sub>TTIA</sub> pins are normally tied to the V <sub>TTIB</sub> pins.                                                                                           |
| H4      | V <sub>EE</sub>         | Power   | Negative Supply.                                                                                                                                                                                    |
| H23     | $\overline{WE}/SCL/SCK$ | Control | Parallel control interface: First-Rank Write Strobe ( $\overline{WE}$ ) Active Low.<br>I <sup>2</sup> C Control Interface: I <sup>2</sup> C Clock (SCL).<br>SPI Control Interface: SPI Clock (SCK). |
| H24     | V <sub>TTIB</sub>       | Power   | Input Termination Supply (B). The V <sub>TTIB</sub> pins are normally tied to the V <sub>TTIA</sub> pins.                                                                                           |

| Pin No. | Mnemonic                    | Type    | Description                                                                                                                                                              |
|---------|-----------------------------|---------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| H25     | IP36                        | Input   | High Speed Input.                                                                                                                                                        |
| H26     | IN35                        | Input   | High Speed Input Complement.                                                                                                                                             |
| J1      | IN5                         | Input   | High Speed Input Complement.                                                                                                                                             |
| J2      | IP6                         | Input   | High Speed Input.                                                                                                                                                        |
| J3      | V <sub>TTIA</sub>           | Power   | Input Termination Supply (A). The V <sub>TTIA</sub> pins are normally tied to the V <sub>TTIB</sub> pins.                                                                |
| J4      | I <sup>2</sup> C/SPI/UPDATE | Control | I <sup>2</sup> C Control Interface Selection (I <sup>2</sup> C).<br>SPI Control Interface Selection (SPI) Active Low.<br>Parallel Control Interface (UPDATE) Active Low. |
| J23     | RE/SDI                      | Control | Parallel Control Interface: Read Strobe (RE) Active Low.<br>SPI Control Interface: Data Input (SDI) SPI Control.                                                         |
| J24     | V <sub>TTIB</sub>           | Power   | Input Termination Supply (B). The V <sub>TTIB</sub> pins are normally tied to the V <sub>TTIA</sub> pins.                                                                |
| J25     | IN34                        | Input   | High Speed Input.                                                                                                                                                        |
| J26     | IP35                        | Input   | High Speed Input Complement.                                                                                                                                             |
| K1      | IP7                         | Input   | High Speed Input.                                                                                                                                                        |
| K2      | IN6                         | Input   | High Speed Input Complement.                                                                                                                                             |
| K3      | V <sub>CC</sub>             | Power   | Power Supply.                                                                                                                                                            |
| K4      | SER/PAR                     | Control | Serial Control Interface Selection (SER).<br>Parallel Control Interface Selection (PAR) Active Low.                                                                      |
| K23     | CS                          | Control | Chip Select Active Low.                                                                                                                                                  |
| K24     | V <sub>CC</sub>             | Power   | Positive Supply.                                                                                                                                                         |
| K25     | IP34                        | Input   | High Speed Input.                                                                                                                                                        |
| K26     | IN33                        | Input   | High Speed Input Complement.                                                                                                                                             |
| L1      | IN7                         | Input   | High Speed Input Complement.                                                                                                                                             |
| L2      | IP8                         | Input   | High Speed Input.                                                                                                                                                        |
| L3      | V <sub>CC</sub>             | Power   | Positive Supply.                                                                                                                                                         |
| L4      | RESET                       | Control | Configuration Registers: Reset (Active Low). This pin is normally pulled up to DV <sub>CC</sub> .                                                                        |
| L23     | DATA0/SDA/SDO               | Control | Parallel Control Interface: Register Data Bit 0 (DATA0).<br>I <sup>2</sup> C Control Interface: Data In (SDA).<br>SPI Control Interface: Data Out (SDO).                 |
| L24     | V <sub>CC</sub>             | Power   | Positive Supply.                                                                                                                                                         |
| L25     | IN32                        | Input   | High Speed Input Complement.                                                                                                                                             |
| L26     | IP33                        | Input   | High Speed Input.                                                                                                                                                        |
| M1      | IP9                         | Input   | High Speed Input.                                                                                                                                                        |
| M2      | IN8                         | Input   | High Speed Input Complement.                                                                                                                                             |
| M3      | V <sub>TTIA</sub>           | Power   | Input Termination Supply (A). The V <sub>TTIA</sub> pins are normally tied to the V <sub>TTIB</sub> pins.                                                                |
| M4      | ADDR0                       | Control | Parallel Control Interface: Register Address Bit 0.<br>I <sup>2</sup> C Control Interface: Slave Address Bit 0.                                                          |
| M23     | DATA1/UPDATE                | Control | Parallel Control Interface: Register (DATA1). Data Bit 1.<br>I <sup>2</sup> C or SPI Serial Control Interface (UPDATE). Active Low.                                      |
| M24     | V <sub>TTIB</sub>           | Power   | Input Termination Supply (B). The V <sub>TTIB</sub> pins are normally tied to the V <sub>TTIA</sub> pins.                                                                |
| M25     | IP32                        | Input   | High Speed Input                                                                                                                                                         |
| M26     | IN31                        | Input   | High Speed Input Complement.                                                                                                                                             |
| N1      | IN9                         | Input   | High Speed Input Complement.                                                                                                                                             |
| N2      | IP10                        | Input   | High Speed Input.                                                                                                                                                        |
| N3      | V <sub>TTIA</sub>           | Power   | Input Termination Supply (A). The V <sub>TTIA</sub> pins are normally tied to the V <sub>TTIB</sub> pins.                                                                |
| N4      | ADDR1                       | Control | Parallel Control Interface: Register Address Bit 1.<br>I <sup>2</sup> C Control Interface: Slave Address Bit 1.                                                          |

| Pin No. | Mnemonic          | Type    | Description                                                                                                     |
|---------|-------------------|---------|-----------------------------------------------------------------------------------------------------------------|
| N23     | DATA2             | Control | Parallel Control Interface: Register Data Bit 2.                                                                |
| N24     | V <sub>TTIB</sub> | Power   | Input Termination Supply (B). The V <sub>TTIB</sub> pins are normally tied to the V <sub>TTIA</sub> pins.       |
| N25     | IN30              | Input   | High Speed Input Complement.                                                                                    |
| N26     | IP31              | Input   | High Speed Input.                                                                                               |
| P1      | IP11              | Input   | High Speed Input.                                                                                               |
| P2      | IN10              | Input   | High Speed Input Complement.                                                                                    |
| P3      | V <sub>TTIA</sub> | Power   | Input Termination Supply (A). The V <sub>TTIA</sub> pins are normally tied to the V <sub>TTIB</sub> pins.       |
| P4      | ADDR2             | Control | Parallel Control Interface: Register Address Bit 2.<br>I <sup>2</sup> C Control Interface: Slave Address Bit 2. |
| P23     | DATA3             | Control | Parallel Control Interface: Register Data Bit 3.                                                                |
| P24     | V <sub>TTIB</sub> | Power   | Input Termination Supply (B). The V <sub>TTIB</sub> pins are normally tied to the V <sub>TTIA</sub> pins.       |
| P25     | IP30              | Input   | High Speed Input.                                                                                               |
| P26     | IN29              | Input   | High Speed Input Complement.                                                                                    |
| R1      | IN11              | Input   | High Speed Input Complement.                                                                                    |
| R2      | IP12              | Input   | High Speed Input.                                                                                               |
| R3      | V <sub>CC</sub>   | Power   | Positive Supply.                                                                                                |
| R4      | ADDR3             | Control | Parallel Control Interface: Register Address Bit 3.<br>I <sup>2</sup> C Control Interface: Slave Address Bit 3. |
| R23     | DATA4             | Control | Parallel Control Interface: Register Data Bit 4.                                                                |
| R24     | V <sub>CC</sub>   | Power   | Positive Supply.                                                                                                |
| R25     | IN28              | Input   | High Speed Input Complement.                                                                                    |
| R26     | IP29              | Input   | High Speed Input.                                                                                               |
| T1      | IP13              | Input   | High Speed Input.                                                                                               |
| T2      | IN12              | Input   | High Speed Input Complement.                                                                                    |
| T3      | V <sub>CC</sub>   | Power   | Positive Supply.                                                                                                |
| T4      | ADDR4             | Control | Parallel Control Interface: Register Address Bit 4.<br>I <sup>2</sup> C Control Interface: Slave Address Bit 4. |
| T23     | DATA5             | Control | Parallel Control Interface: Register Data Bit 5.                                                                |
| T24     | V <sub>CC</sub>   | Power   | Positive Supply.                                                                                                |
| T25     | IP28              | Input   | High Speed Input.                                                                                               |
| T26     | IN27              | Input   | High Speed Input Complement.                                                                                    |
| U1      | IN13              | Input   | High Speed Input Complement.                                                                                    |
| U2      | IP14              | Input   | High Speed Input.                                                                                               |
| U3      | V <sub>TTIA</sub> | Power   | Input Termination Supply (A). The V <sub>TTIA</sub> pins are normally tied to the V <sub>TTIB</sub> pins.       |
| U4      | ADDR5             | Control | Parallel Control Interface: Register Address Bit 5.<br>I <sup>2</sup> C Control Interface: Slave Address Bit 5. |
| U23     | DATA6             | Control | Parallel Control Interface: Register Data Bit 6.                                                                |
| U24     | V <sub>TTIB</sub> | Power   | Input Termination Supply (B). The V <sub>TTIB</sub> pins are normally tied to the V <sub>TTIA</sub> pins.       |
| U25     | IN26              | Input   | High Speed Input Complement.                                                                                    |
| U26     | IP27              | Input   | High Speed Input.                                                                                               |
| V1      | IP15              | Input   | High Speed Input.                                                                                               |
| V2      | IN14              | Input   | High Speed Input Complement.                                                                                    |
| V3      | V <sub>TTIA</sub> | Power   | Input Termination Supply (A). The V <sub>TTIA</sub> pins are normally tied to the V <sub>TTIB</sub> pins.       |
| V4      | ADDR6             | Control | Parallel Control Interface: Register Address Bit 6.<br>I <sup>2</sup> C Control Interface: Slave Address Bit 6. |
| V23     | DATA7             | Control | Parallel Control Interface: Register Data Bit 7.                                                                |

| Pin No. | Mnemonic          | Type    | Description                                                                                                     |
|---------|-------------------|---------|-----------------------------------------------------------------------------------------------------------------|
| V24     | V <sub>TTIB</sub> | Power   | Input Termination Supply (B). The V <sub>TTIB</sub> pins are normally tied to the V <sub>TTIA</sub> pins.       |
| V25     | IP26              | Input   | High Speed Input.                                                                                               |
| V26     | IN25              | Input   | High Speed Input Complement.                                                                                    |
| W1      | IN15              | Input   | High Speed Input Complement.                                                                                    |
| W2      | IP16              | Input   | High Speed Input.                                                                                               |
| W3      | V <sub>TTIA</sub> | Power   | Input Termination Supply (A). The V <sub>TTIA</sub> pins are normally tied to the V <sub>TTIB</sub> pins.       |
| W4      | ADDR7             | Control | Parallel Control Interface: Register Address Bit 7.<br>I <sup>2</sup> C Control Interface: Slave Address Bit 7. |
| W23     | V <sub>EE</sub>   | Power   | Negative Supply.                                                                                                |
| W24     | V <sub>TTIB</sub> | Power   | Input Termination Supply (B). The V <sub>TTIB</sub> pins are normally tied to the V <sub>TTIA</sub> pins.       |
| W25     | IN24              | Input   | High Speed Input Complement.                                                                                    |
| W26     | IP25              | Input   | High Speed Input.                                                                                               |
| Y1      | IP17              | Input   | High Speed Input.                                                                                               |
| Y2      | IN16              | Input   | High Speed Input Complement.                                                                                    |
| Y3      | V <sub>TTIA</sub> | Power   | Input Termination Supply (A). The V <sub>TTIA</sub> pins are normally tied to the V <sub>TTIB</sub> pins.       |
| Y4      | V <sub>EE</sub>   | Power   | Negative Supply.                                                                                                |
| Y23     | V <sub>EE</sub>   | Power   | Negative Supply.                                                                                                |
| Y24     | V <sub>TTIB</sub> | Power   | Input Termination Supply (B). The V <sub>TTIB</sub> pins are normally tied to the V <sub>TTIA</sub> pins.       |
| Y25     | IP24              | Input   | High Speed Input.                                                                                               |
| Y26     | IN23              | Input   | High Speed Input Complement.                                                                                    |
| AA1     | IN17              | Input   | High Speed Input Complement.                                                                                    |
| AA2     | IP18              | Input   | High Speed Input.                                                                                               |
| AA3     | V <sub>CC</sub>   | Power   | Positive Supply.                                                                                                |
| AA4     | V <sub>EE</sub>   | Power   | Negative Supply.                                                                                                |
| AA23    | V <sub>EE</sub>   | Power   | Negative Supply.                                                                                                |
| AA24    | V <sub>CC</sub>   | Power   | Positive Supply.                                                                                                |
| AA25    | IN22              | Input   | High Speed Input Complement.                                                                                    |
| AA26    | IP23              | Input   | High Speed Input.                                                                                               |
| AB1     | IP19              | Input   | High Speed Input.                                                                                               |
| AB2     | IN18              | Input   | High Speed Input Complement.                                                                                    |
| AB3     | V <sub>CC</sub>   | Power   | Positive Supply.                                                                                                |
| AB4     | V <sub>EE</sub>   | Power   | Negative Supply.                                                                                                |
| AB23    | V <sub>EE</sub>   | Power   | Negative Supply.                                                                                                |
| AB24    | V <sub>CC</sub>   | Power   | Positive Supply.                                                                                                |
| AB25    | IP22              | Input   | High Speed Input.                                                                                               |
| AB26    | IN21              | Input   | High Speed Input Complement.                                                                                    |
| AC1     | IN19              | Input   | High Speed Input Complement.                                                                                    |
| AC2     | V <sub>EE</sub>   | Power   | Negative Supply.                                                                                                |
| AC3     | V <sub>CC</sub>   | Power   | Positive Supply.                                                                                                |
| AC4     | DV <sub>CC</sub>  | Power   | Digital Positive Supply.                                                                                        |
| AC5     | V <sub>CC</sub>   | Power   | Positive Supply.                                                                                                |
| AC6     | V <sub>CC</sub>   | Power   | Positive Supply.                                                                                                |
| AC7     | V <sub>EE</sub>   | Power   | Negative Supply.                                                                                                |
| AC8     | V <sub>EE</sub>   | Power   | Negative Supply.                                                                                                |
| AC9     | V <sub>EE</sub>   | Power   | Negative Supply.                                                                                                |
| AC10    | V <sub>EE</sub>   | Power   | Negative Supply.                                                                                                |

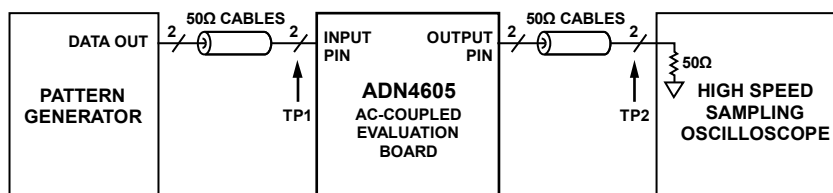
| Pin No. | Mnemonic          | Type  | Description                                                                                                |
|---------|-------------------|-------|------------------------------------------------------------------------------------------------------------|
| AC11    | V <sub>CC</sub>   | Power | Positive Supply.                                                                                           |
| AC12    | V <sub>CC</sub>   | Power | Positive Supply.                                                                                           |
| AC13    | V <sub>EE</sub>   | Power | Negative Supply.                                                                                           |
| AC14    | V <sub>EE</sub>   | Power | Negative Supply.                                                                                           |
| AC15    | V <sub>EE</sub>   | Power | Negative Supply.                                                                                           |
| AC16    | V <sub>CC</sub>   | Power | Positive Supply.                                                                                           |
| AC17    | V <sub>CC</sub>   | Power | Positive Supply.                                                                                           |
| AC18    | V <sub>EE</sub>   | Power | Negative Supply.                                                                                           |
| AC19    | V <sub>EE</sub>   | Power | Negative Supply.                                                                                           |
| AC20    | V <sub>EE</sub>   | Power | Negative Supply.                                                                                           |
| AC21    | V <sub>EE</sub>   | Power | Negative Supply.                                                                                           |
| AC22    | V <sub>CC</sub>   | Power | Positive Supply.                                                                                           |
| AC23    | DV <sub>CC</sub>  | Power | Digital Positive Supply.                                                                                   |
| AC24    | V <sub>CC</sub>   | Power | Positive Supply.                                                                                           |
| AC25    | IN20              | Input | High Speed Input Complement.                                                                               |
| AC26    | IP21              | Input | High Speed Input.                                                                                          |
| AD1     | V <sub>EE</sub>   | Power | Negative Supply.                                                                                           |
| AD2     | V <sub>EE</sub>   | Power | Negative Supply.                                                                                           |
| AD3     | V <sub>EE</sub>   | Power | Negative Supply.                                                                                           |
| AD4     | V <sub>CC</sub>   | Power | Positive Supply.                                                                                           |
| AD5     | V <sub>CC</sub>   | Power | Positive Supply.                                                                                           |
| AD6     | V <sub>CC</sub>   | Power | Positive Supply.                                                                                           |
| AD7     | V <sub>TTOA</sub> | Power | Output Termination Supply (A). The V <sub>TTOA</sub> pins are normally tied to the V <sub>TTOB</sub> pins. |
| AD8     | V <sub>TTOA</sub> | Power | Output Termination Supply (A). The V <sub>TTOA</sub> pins are normally tied to the V <sub>TTOB</sub> pins. |
| AD9     | V <sub>TTOA</sub> | Power | Output Termination Supply (A). The V <sub>TTOA</sub> pins are normally tied to the V <sub>TTOB</sub> pins. |
| AD10    | V <sub>TTOA</sub> | Power | Output Termination Supply (A). The V <sub>TTOA</sub> pins are normally tied to the V <sub>TTOB</sub> pins. |
| AD11    | V <sub>CC</sub>   | Power | Positive Supply.                                                                                           |
| AD12    | V <sub>CC</sub>   | Power | Positive Supply.                                                                                           |
| AD13    | V <sub>TTOA</sub> | Power | Output Termination Supply (A). The V <sub>TTOA</sub> pins are normally tied to the V <sub>TTOB</sub> pins. |
| AD14    | V <sub>TTOA</sub> | Power | Output Termination Supply (A). The V <sub>TTOA</sub> pins are normally tied to the V <sub>TTOB</sub> pins. |
| AD15    | V <sub>TTOA</sub> | Power | Output Termination Supply (A). The V <sub>TTOA</sub> pins are normally tied to the V <sub>TTOB</sub> pins. |
| AD16    | V <sub>CC</sub>   | Power | Positive Supply.                                                                                           |
| AD17    | V <sub>CC</sub>   | Power | Positive Supply.                                                                                           |
| AD18    | V <sub>TTOA</sub> | Power | Output Termination Supply (A). The V <sub>TTOA</sub> pins are normally tied to the V <sub>TTOB</sub> pins. |
| AD19    | V <sub>TTOA</sub> | Power | Output Termination Supply (A). The V <sub>TTOA</sub> pins are normally tied to the V <sub>TTOB</sub> pins. |
| AD20    | V <sub>TTOA</sub> | Power | Output Termination Supply (A). The V <sub>TTOA</sub> pins are normally tied to the V <sub>TTOB</sub> pins. |
| AD21    | V <sub>TTOA</sub> | Power | Output Termination Supply (A). The V <sub>TTOA</sub> pins are normally tied to the V <sub>TTOB</sub> pins. |
| AD22    | V <sub>CC</sub>   | Power | Positive Supply.                                                                                           |
| AD23    | V <sub>CC</sub>   | Power | Positive Supply.                                                                                           |
| AD24    | V <sub>EE</sub>   | Power | Negative Supply.                                                                                           |
| AD25    | IP20              | Input | High Speed Input.                                                                                          |
| AD26    | V <sub>EE</sub>   | Power | Negative Supply.                                                                                           |

| Pin No. | Mnemonic        | Type   | Description                   |
|---------|-----------------|--------|-------------------------------|
| AE1     | V <sub>EE</sub> | Power  | Negative Supply.              |
| AE2     | V <sub>EE</sub> | Power  | Negative Supply.              |
| AE3     | OP0             | Output | High Speed Output.            |
| AE4     | ON0             | Output | High Speed Output Complement. |
| AE5     | OP2             | Output | High Speed Output.            |
| AE6     | ON2             | Output | High Speed Output Complement. |
| AE7     | OP4             | Output | High Speed Output.            |
| AE8     | ON4             | Output | High Speed Output Complement. |
| AE9     | OP6             | Output | High Speed Output.            |
| AE10    | ON6             | Output | High Speed Output Complement. |
| AE11    | OP8             | Output | High Speed Output.            |
| AE12    | ON8             | Output | High Speed Output Complement. |
| AE13    | OP10            | Output | High Speed Output.            |
| AE14    | ON10            | Output | High Speed Output Complement. |
| AE15    | OP12            | Output | High Speed Output.            |
| AE16    | ON12            | Output | High Speed Output Complement. |
| AE17    | OP14            | Output | High Speed Output.            |
| AE18    | ON14            | Output | High Speed Output Complement. |
| AE19    | OP16            | Output | High Speed Output.            |
| AE20    | ON16            | Output | High Speed Output Complement. |
| AE21    | OP18            | Output | High Speed Output.            |
| AE22    | ON18            | Output | High Speed Output Complement. |
| AE23    | V <sub>EE</sub> | Power  | Negative Supply.              |
| AE24    | V <sub>EE</sub> | Power  | Negative Supply.              |
| AE25    | V <sub>EE</sub> | Power  | Negative Supply.              |
| AE26    | V <sub>EE</sub> | Power  | Negative Supply.              |
| AF1     | V <sub>EE</sub> | Power  | Negative Supply.              |
| AF2     | V <sub>EE</sub> | Power  | Negative Supply.              |
| AF3     | V <sub>EE</sub> | Power  | Negative Supply.              |
| AF4     | OP1             | Output | High Speed Output.            |
| AF5     | ON1             | Output | High Speed Output Complement. |
| AF6     | OP3             | Output | High Speed Output.            |
| AF7     | ON3             | Output | High Speed Output Complement. |
| AF8     | OP5             | Output | High Speed Output.            |
| AF9     | ON5             | Output | High Speed Output Complement. |
| AF10    | OP7             | Output | High Speed Output.            |
| AF11    | ON7             | Output | High Speed Output Complement. |
| AF12    | OP9             | Output | High Speed Output.            |
| AF13    | ON9             | Output | High Speed Output Complement. |
| AF14    | OP11            | Output | High Speed Output.            |
| AF15    | ON11            | Output | High Speed Output Complement. |
| AF16    | OP13            | Output | High Speed Output.            |
| AF17    | ON13            | Output | High Speed Output Complement. |
| AF18    | OP15            | Output | High Speed Output.            |
| AF19    | ON15            | Output | High Speed Output Complement. |
| AF20    | OP17            | Output | High Speed Output.            |
| AF21    | ON17            | Output | High Speed Output Complement. |
| AF22    | OP19            | Output | High Speed Output.            |

| Pin No. | Mnemonic        | Type   | Description                   |
|---------|-----------------|--------|-------------------------------|
| AF23    | ON19            | Output | High Speed Output Complement. |
| AF24    | V <sub>EE</sub> | Power  | Negative Supply.              |
| AF25    | V <sub>EE</sub> | Power  | Negative Supply.              |
| AF26    | V <sub>EE</sub> | Power  | Negative Supply.              |

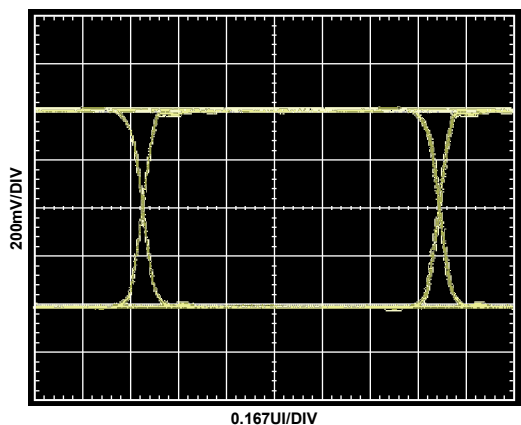
## TYPICAL PERFORMANCE CHARACTERISTICS

$V_{CC} = 2.5$  V,  $V_{TTk} = 2.5$  V,  $V_{TTox} = 2.5$  V,  $DV_{CC} = 3.3$  V,  $V_{EE} = 0$  V,  $R_L = 50$   $\Omega$ , output level (OLEV) = 4 (16 mA), preemphasis (PE) = 0 (0 dB), equalizer (EQ) = 1 (3 dB), data rate = 4.25 Gbps (PRBS7 data pattern), ac-coupled inputs and outputs, differential input swing = 800 mV p-p,  $T_A = 25^\circ\text{C}$ , unless otherwise noted.



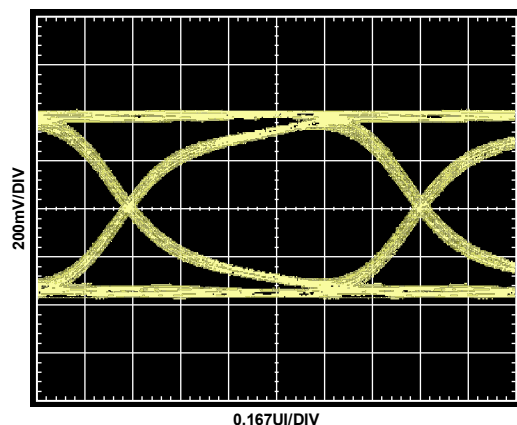
09796-048

Figure 7. Standard Test Circuit



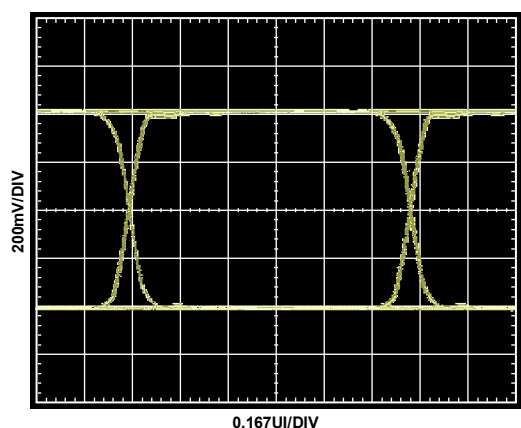
09796-035

Figure 8. 3.25 Gbps Input Eye (TP1 from Figure 7)



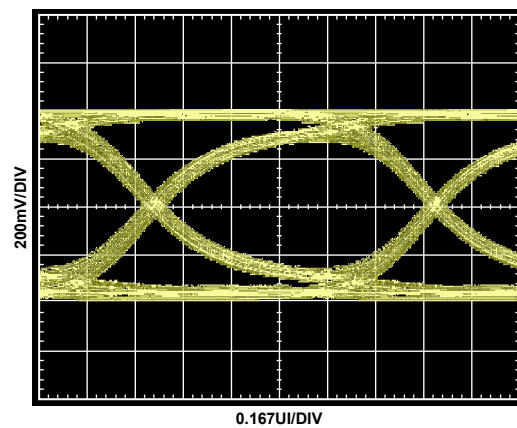
09796-034

Figure 10. 3.25 Gbps Output Eye (TP2 from Figure 7)



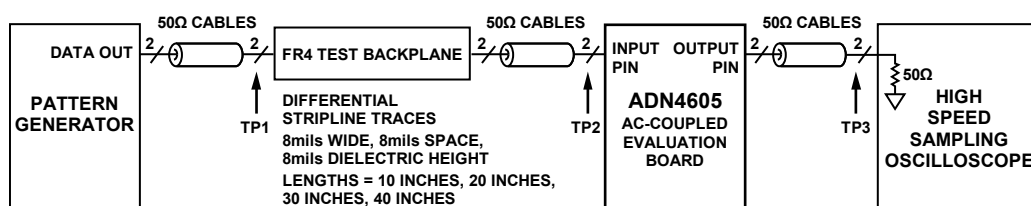
09796-047

Figure 9. 4.25 Gbps Input Eye (TP1 from Figure 7)



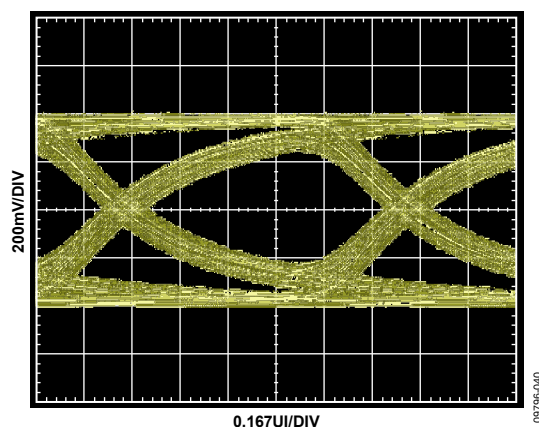
09796-046

Figure 11. 4.25 Gbps Output Eye (TP2 from Figure 7)



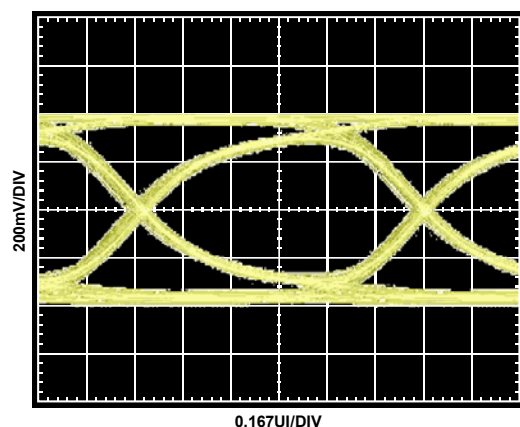
09796-049

Figure 12. Equalization Test Circuit



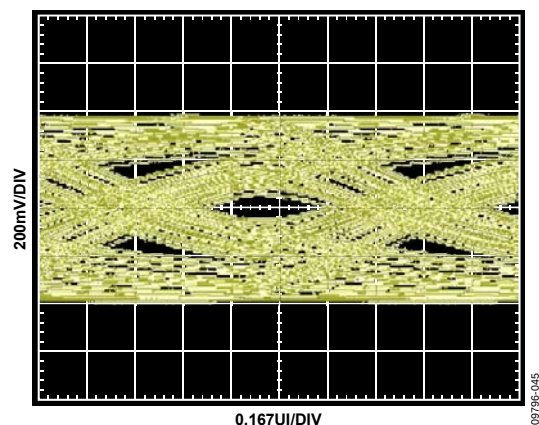
09796-040

Figure 13. 4.25 Gbps Input Eye, 20-Inch FR4 Input Channel (TP2 from Figure 12)



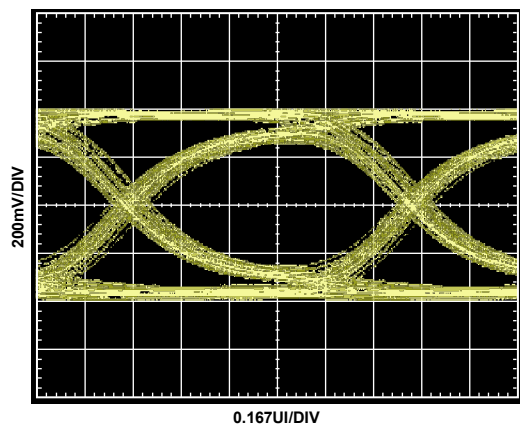
09796-038

Figure 15. 4.25 Gbps Output Eye, 20-Inch FR4 Input Channel, EQ = 12 dB (TP3 from Figure 12)



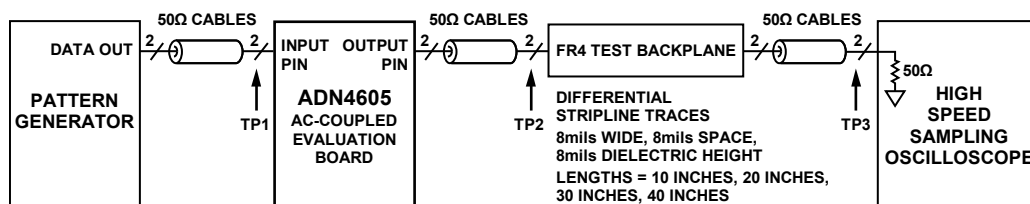
09796-045

Figure 14. 4.25 Gbps Input Eye, 40-Inch FR4 Input Channel (TP2 from Figure 12)



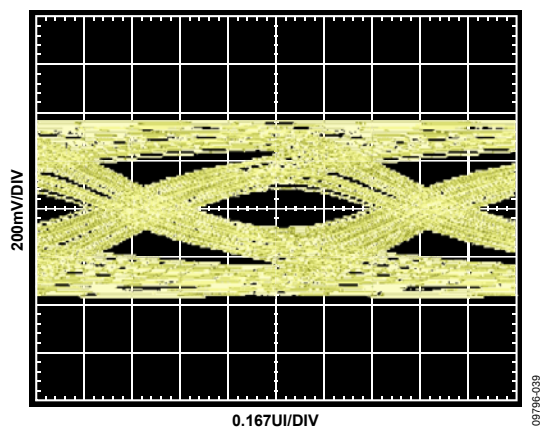
09796-043

Figure 16. 4.25 Gbps Output Eye, 40-Inch FR4 Input Channel, EQ = 12 dB (TP3 from Figure 12)



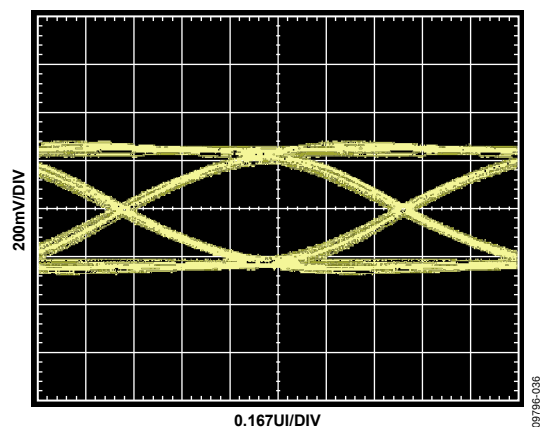
09796-050

Figure 17. Preemphasis Test Circuit



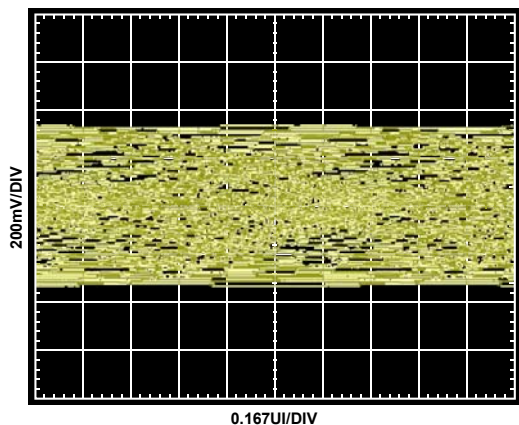
09796-039

Figure 18. 4.25 Gbps Output Eye, 20-Inch FR4 Output Channel, PE = 0 dB (TP3 from Figure 17)



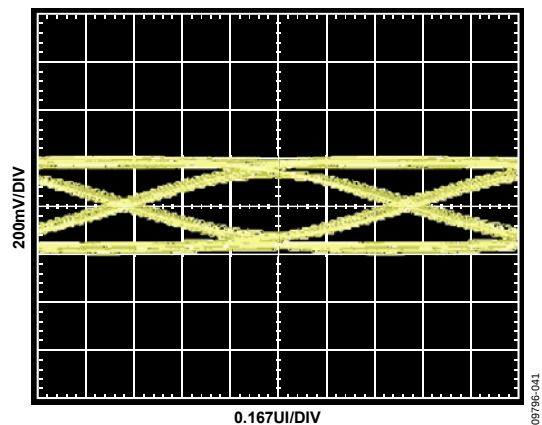
09796-036

Figure 20. 4.25 Gbps Output Eye, 20-Inch FR4 Input Channel, PE = 5.6 dB (TP3 from Figure 17)



09796-044

Figure 19. 4.25 Gbps Output Eye, 40-Inch FR4 Input Channel, PE = 0 dB (TP3 from Figure 17)



09796-041

Figure 21. 4.25 Gbps Output Eye, 40-Inch FR4 Input Channel, PE = 9.5 dB (TP3 from Figure 17)

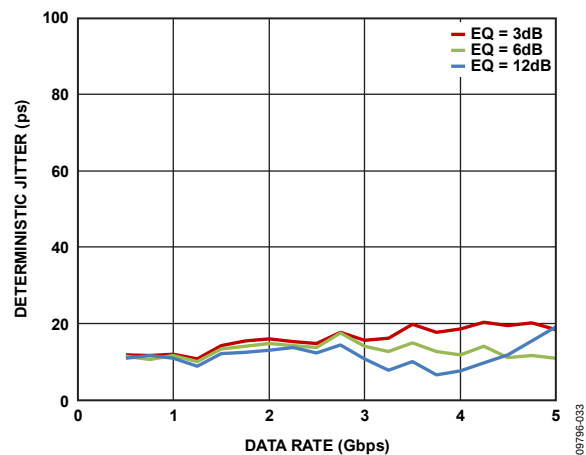


Figure 22. Deterministic Jitter vs. Data Rate

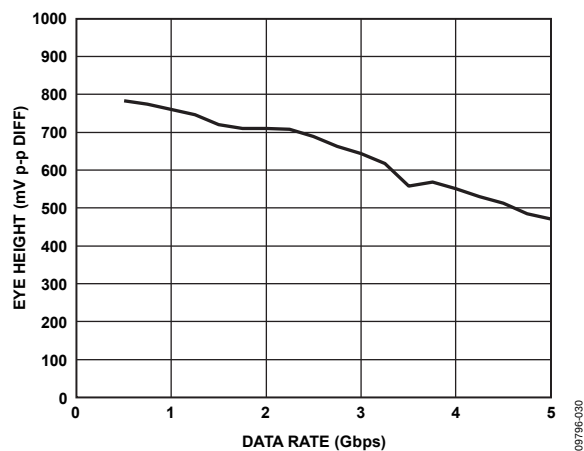


Figure 25. Eye Height vs. Data Rate

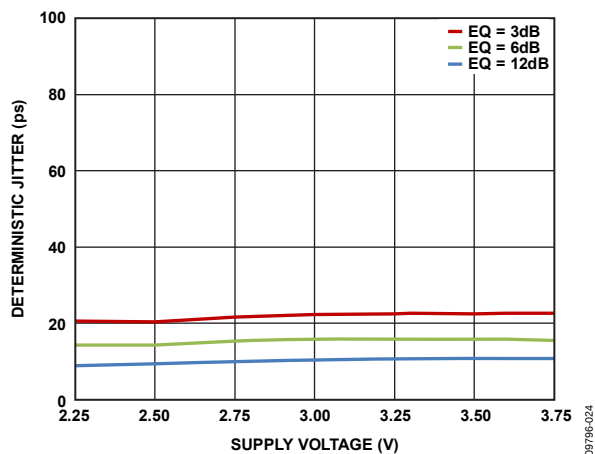


Figure 23. Deterministic Jitter vs. Supply Voltage

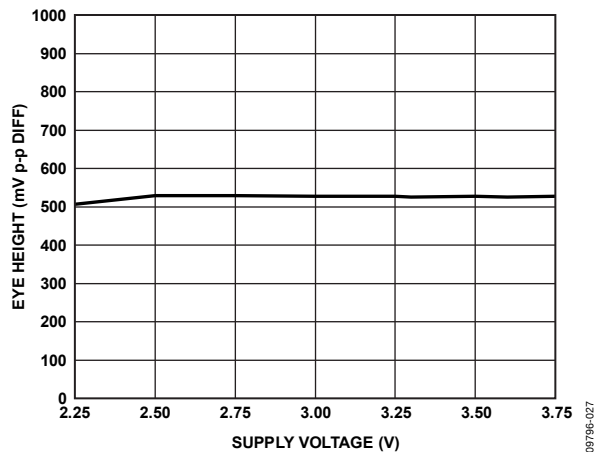


Figure 26. Eye Height vs. Supply Voltage

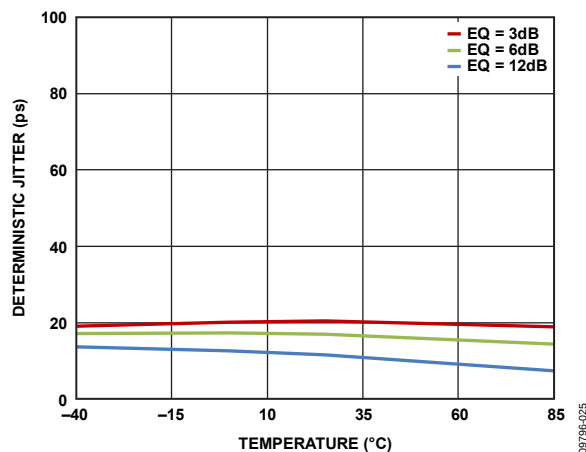


Figure 24. Deterministic Jitter vs. Temperature

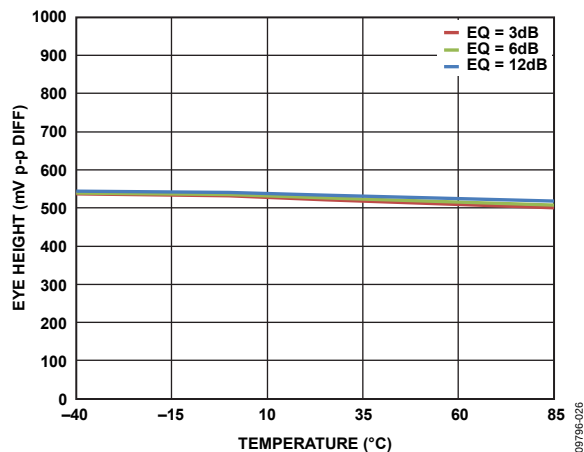


Figure 27. Eye Height vs. Temperature

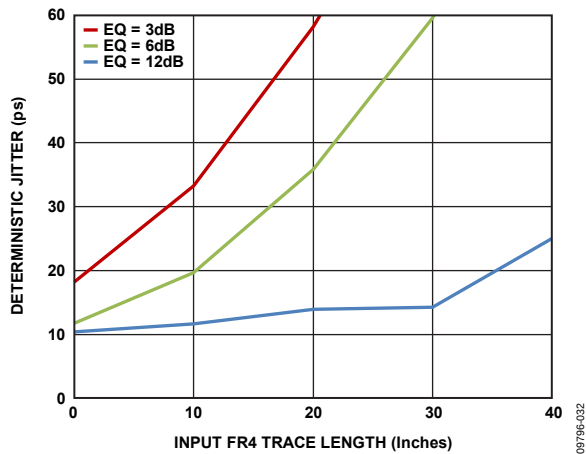


Figure 28. Deterministic Jitter vs. Input FR4 Channel Length

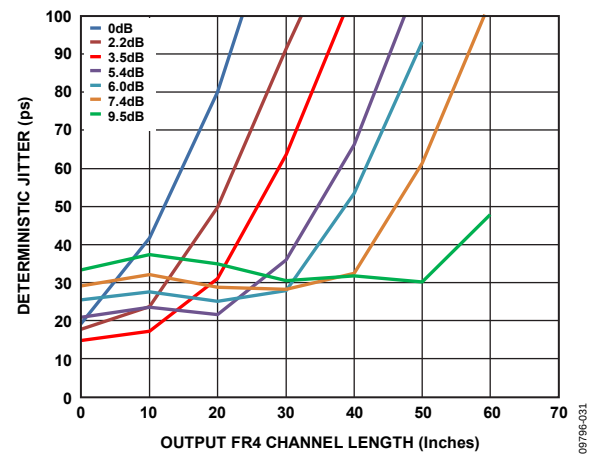


Figure 31. Deterministic Jitter vs. Output FR4 Channel Length

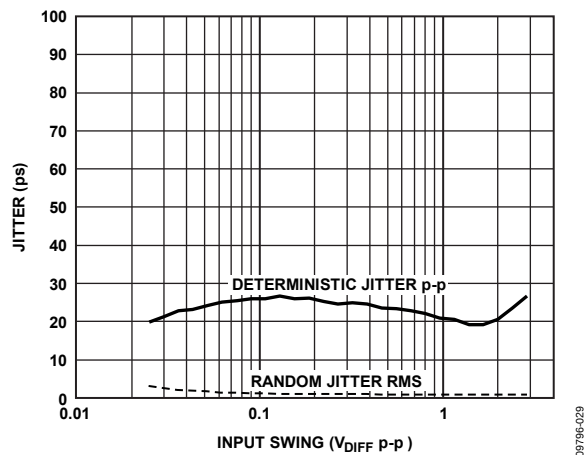


Figure 29. Jitter vs. Differential Input Swing

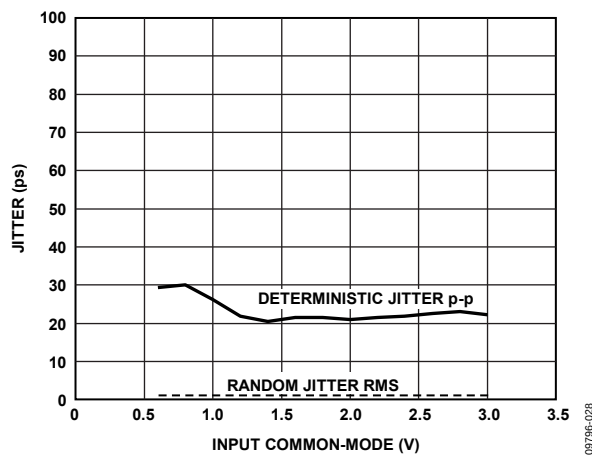


Figure 32. Jitter vs. Input Common-Mode Voltage

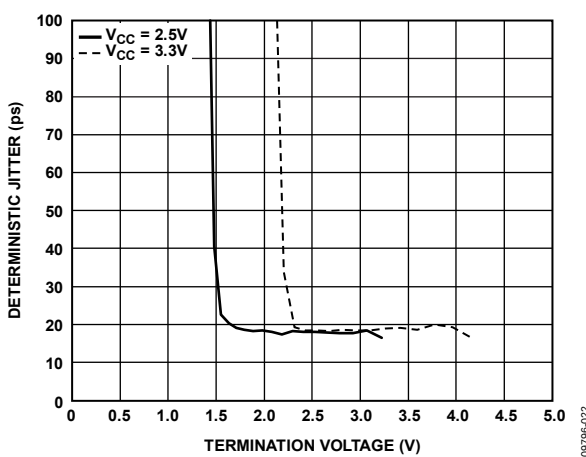
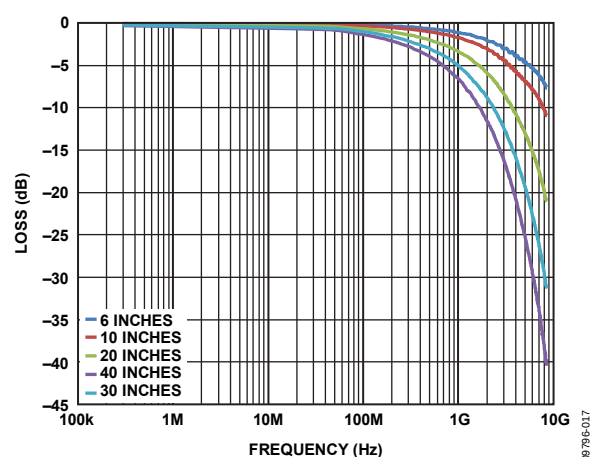
Figure 30. Deterministic Jitter vs. Output Termination Voltage ( $V_{TIO}$ )

Figure 33. S21 Test Traces

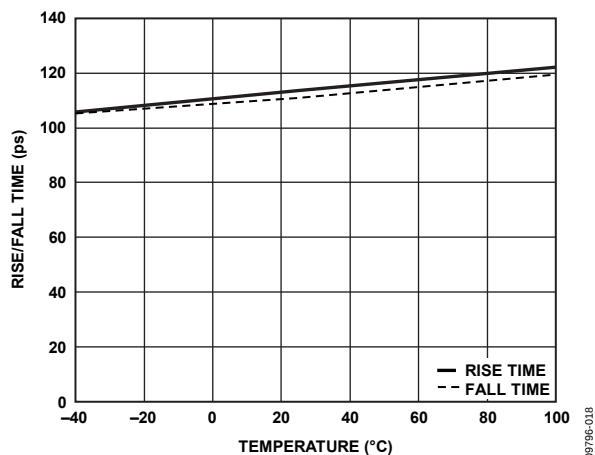


Figure 34. Rise/Fall Time vs. Temperature

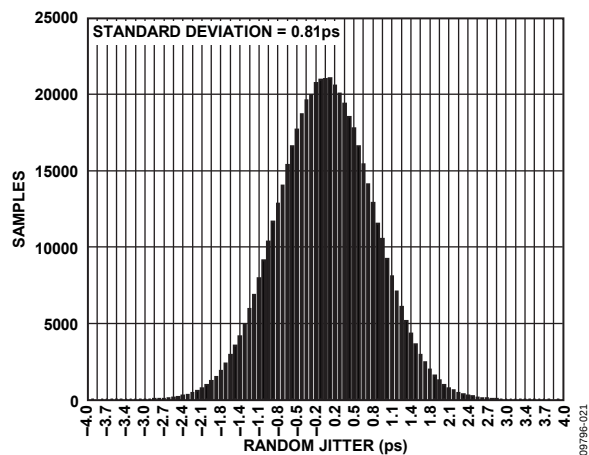


Figure 37. Random Jitter Histogram

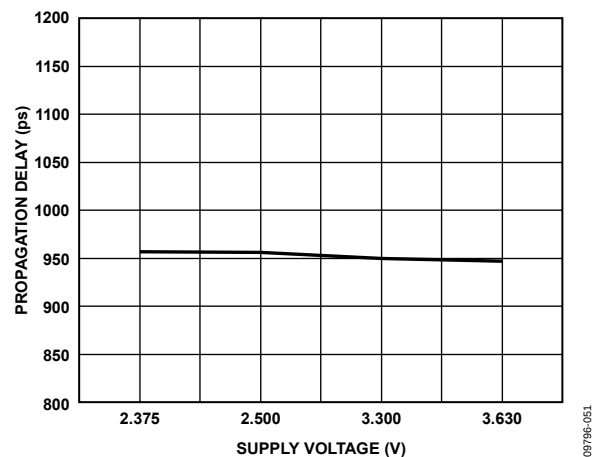


Figure 35. Propagation Delay vs. Supply Voltage

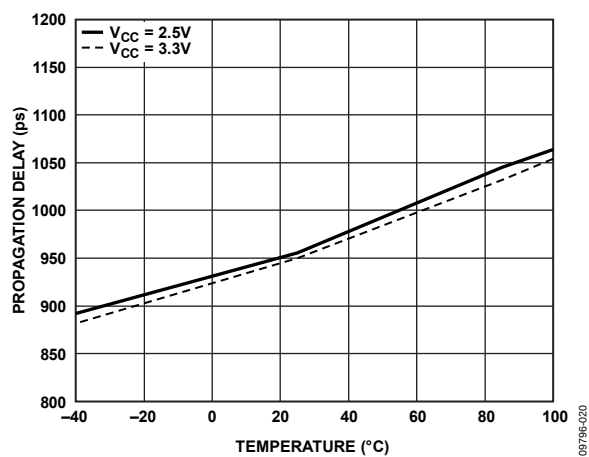


Figure 38. Propagation Delay vs. Temperature

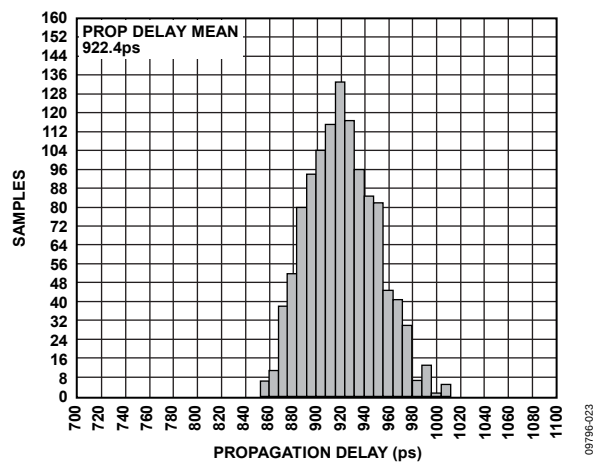


Figure 36. Propagation Delay Histogram

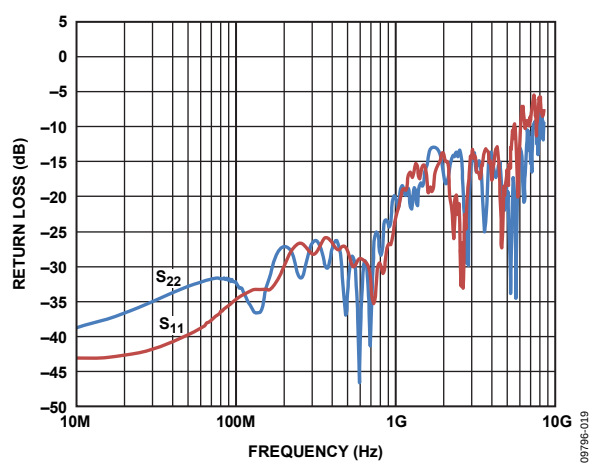


Figure 39. Return Loss (S11, S22)

## THEORY OF OPERATION

### INTRODUCTION

The ADN4605 is a  $40 \times 40$ , buffered, asynchronous crosspoint switch that provides input equalization, output preemphasis, and output level programming capabilities. The receivers integrate an equalizer that is optimized to compensate for typical backplane losses. The switch supports multicast and broadcast operation, allowing the ADN4605 to work in redundancy and port replication applications.

The ADN4605 is configured through either the serial or parallel control interface. The serial or parallel control interface is selected using the SER/PAR dedicated control pin. The serial interface supports both I<sup>2</sup>C and SPI protocols selected using the I<sup>2</sup>C/SPI dedicated control pin. The ADN4605 control pins function differently depending on which programming interface is selected, as described in Table 9.

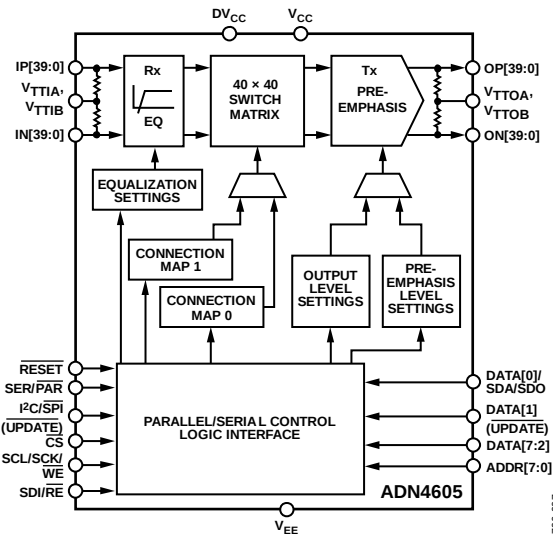


Figure 40. Block Diagram

Table 9. Parallel/Serial Interface Pin Control

| Pin No.                      | Pin Name                    | Parallel Mode<br>(SER/PAR = 0)              | I <sup>2</sup> C Mode<br>(SER/PAR = 1, I <sup>2</sup> C/SPI = 1)           | SPI Mode<br>(SER/PAR = 1, I <sup>2</sup> C/SPI = 0) |
|------------------------------|-----------------------------|---------------------------------------------|----------------------------------------------------------------------------|-----------------------------------------------------|
|                              |                             | Pin Function                                | Pin Function                                                               | Pin Function                                        |
| K4                           | SER/PAR                     | Serial/parallel control interface selection | Serial/parallel control interface selection                                | Serial/parallel control interface selection         |
| J4                           | I <sup>2</sup> C/SPI/UPDATE | Update strobe                               | I <sup>2</sup> C/SPI control interface selection                           | I <sup>2</sup> C/SPI control interface selection    |
| H23                          | WE/SCL/SCK                  | Parallel write strobe                       | I <sup>2</sup> C clock                                                     | SPI clock                                           |
| J23                          | RE/SDI                      | Parallel read strobe                        | N/A                                                                        | SPI data input                                      |
| K23                          | CS                          | Chip select                                 | N/A                                                                        | Chip select                                         |
| L23                          | DATA0/SDA/SDO               | Parallel register data bit (LSB)            | I <sup>2</sup> C data input                                                | SPI data output                                     |
| M23                          | DATA1/UPDATE                | Parallel register data bits                 | Update strobe                                                              | Update strobe                                       |
| N23, P23, R23, T23, U23, V23 | DATA2 to DATA7              | Parallel register data bits                 | N/A                                                                        | N/A                                                 |
| L4                           | RESET                       | Device register reset (active low)          | Device register reset (active low)                                         | Device register reset (active low)                  |
| M4                           | ADDR0                       | Parallel register address bit (LSB)         | N/A                                                                        | N/A                                                 |
| N4, P4, R4, T4, U4, V4, W4   | ADDR1 to ADDR7              | Parallel register address bits              | I <sup>2</sup> C LSB device address to I <sup>2</sup> C MSB device address | N/A                                                 |

## RECEIVERS

### Input Structure and Input Levels

The ADN4605 receiver inputs incorporate 50  $\Omega$  termination resistors, ESD protection, and a fixed equalizer that is optimized for operation over long backplane traces. Each receive channel also provides a positive/negative (P/N) inversion function, which allows the user to swap the sign of the input signal path to eliminate the need for board-level crossovers.

### Equalization

The ADN4605 receiver incorporates a continuous time equalizer (EQ) that provides up to 12 dB of high frequency boost to compensate up to 40 inches of FR4 at 4.25 Gbps. Each input has two equalizer control bits. The receiver is disabled by default. The boost can be set to defined levels by programming the respective address register bits (Address 0xC0 through Address 0xC9) for the target input channel to the specified logic combinations as shown in Table 10.

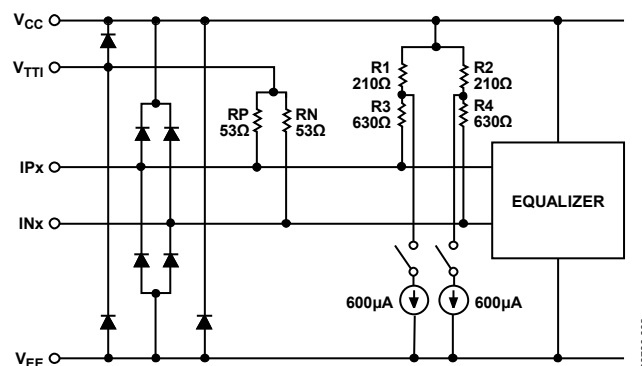


Figure 41. Simplified Input Circuit

Table 10. Equalization Control Registers

| Register Address | Default | Register Name                           | Bits                     | Bit Name                                                 | Functionality Description                                                            |
|------------------|---------|-----------------------------------------|--------------------------|----------------------------------------------------------|--------------------------------------------------------------------------------------|
| 0xC0             | 0x0     | Rx EQ Control<br>(Rx IN 3 to Rx IN 0)   | 7:6<br>5:4<br>3:2<br>1:0 | RXEQIN [3]<br>RXEQIN [2]<br>RXEQIN [1]<br>RXEQIN [0]     | 00 = Rx disabled (default)<br>01 = 3 dB boost<br>10 = 6 dB boost<br>11 = 12 dB boost |
| 0xC1             | 0x0     | Rx EQ Control<br>(Rx IN 7 to Rx IN 4)   | 7:6<br>5:4<br>3:2<br>1:0 | RXEQIN [7]<br>RXEQIN [6]<br>RXEQIN [5]<br>RXEQIN [4]     |                                                                                      |
| 0xC2             | 0x0     | Rx EQ Control<br>(Rx IN 11 to Rx IN 8)  | 7:6<br>5:4<br>3:2<br>1:0 | RXEQIN [11]<br>RXEQIN [10]<br>RXEQIN [9]<br>RXEQIN [8]   |                                                                                      |
| 0xC3             | 0x0     | Rx EQ Control<br>(Rx IN 15 to Rx IN 12) | 7:6<br>5:4<br>3:2<br>1:0 | RXEQIN [15]<br>RXEQIN [14]<br>RXEQIN [13]<br>RXEQIN [12] |                                                                                      |
| 0xC4             | 0x0     | Rx EQ Control<br>(Rx IN 19 to Rx IN 16) | 7:6<br>5:4<br>3:2<br>1:0 | RXEQIN [19]<br>RXEQIN [18]<br>RXEQIN [17]<br>RXEQIN [16] |                                                                                      |
| 0xC5             | 0x0     | Rx EQ Control<br>(Rx IN 23 to Rx IN 20) | 7:6<br>5:4<br>3:2<br>1:0 | RXEQIN [23]<br>RXEQIN [22]<br>RXEQIN [21]<br>RXEQIN [20] |                                                                                      |
| 0xC6             | 0x0     | Rx EQ Control<br>(Rx IN 27 to Rx IN 24) | 7:6<br>5:4<br>3:2<br>1:0 | RXEQIN [27]<br>RXEQIN [26]<br>RXEQIN [25]<br>RXEQIN [24] |                                                                                      |

| Register Address | Default             | Register Name                           | Bits                     | Bit Name                                                 | Functionality Description                                                            |
|------------------|---------------------|-----------------------------------------|--------------------------|----------------------------------------------------------|--------------------------------------------------------------------------------------|
| 0xC7             | 0x0                 | Rx EQ Control<br>(Rx IN 31 to Rx IN 28) | 7:6<br>5:4<br>3:2<br>1:0 | RXEQIN [31]<br>RXEQIN [30]<br>RXEQIN [29]<br>RXEQIN [28] | 00 = Rx disabled (default)<br>01 = 3 dB boost<br>10 = 6 dB boost<br>11 = 12 dB boost |
| 0xC8             | 0x0                 | Rx EQ Control<br>(Rx IN35 to Rx IN 32)  | 7:6<br>5:4<br>3:2<br>1:0 | RXEQIN [35]<br>RXEQIN [34]<br>RXEQIN [33]<br>RXEQIN [32] |                                                                                      |
| 0xC9             | 0x0                 | Rx EQ Control<br>(Rx IN 39 to Rx IN 36) | 7:6<br>5:4<br>3:2<br>1:0 | RXEQIN [39]<br>RXEQIN [38]<br>RXEQIN [37]<br>RXEQIN [36] |                                                                                      |
| 0xCA             | 0x0<br>(Write only) | Rx EQ Control<br>(Rx IN Broadcast)      | 1:0                      | RXEQIN BC                                                |                                                                                      |

## POLARITY INVERSION

The P/N inversion is a feature intended to allow the user to implement the equivalent of a board-level crossover in a much smaller area and without additional via impedance discontinuities that degrade the high frequency integrity of the signal path. The P/N inversion is available independently for each of the 40 input and output channels, which are controlled by writing to the RXSIGN bit of the RX Sign control registers (Addresses 0xCB through Address 0xCF) and the TXSIGN bit of the TX control registers (Address 0xA9 through Address 0xAD).

**Table 11. Signal Path Polarity Control**

| Register Address | Default | Register Name                     | Bits | Bit Name                   | Functionality Description                                                    |
|------------------|---------|-----------------------------------|------|----------------------------|------------------------------------------------------------------------------|
| 0xCB             | 0x00    | RX SIGN<br>RX IN 07 to RX IN 00   | 7: 0 | RXSIGN [7]to RXSIGN [0]    | Signal path polarity inversion (input/output)<br>0 = noninvert<br>1 = invert |
| 0xCC             | 0x00    | RX SIGN<br>RX IN 15 to RX IN 08   | 7: 0 | RXSIGN [15] to RXSIGN [8]  |                                                                              |
| 0xCD             | 0x00    | RX SIGN<br>RX IN 23 to RX IN 16   | 7: 0 | RXSIGN[23] to RXSIGN [16]  |                                                                              |
| 0xCE             | 0x00    | RX SIGN<br>RX IN31 to RX IN 24    | 7: 0 | RXSIGN [31] to RXSIGN [24] |                                                                              |
| 0xCF             | 0x00    | RX SIGN<br>RX IN 39 to RX IN 32   | 7: 0 | RXSIGN [39] to RXSIGN [32] |                                                                              |
| 0xA9             | 0x00    | TX SIGN<br>TX OUT 07 to TX OUT 00 | 7: 0 | TXSIGN [7] to TXSIGN [0]   |                                                                              |
| 0xAA             | 0x00    | TX SIGN<br>TX OUT 15 to TX OUT 08 | 7: 0 | TXSIGN [15] to TXSIGN [8]  |                                                                              |
| 0xAB             | 0x00    | TX SIGN<br>TX OUT 23 to TX OUT 16 | 7: 0 | TXSIGN [23] to TXSIGN [16] |                                                                              |
| 0xAC             | 0x00    | TX SIGN<br>TX OUT 31 to TX OUT 24 | 7: 0 | TXSIGN [31] to TXSIGN [24] |                                                                              |
| 0xAD             | 0x00    | TX SIGN<br>TX OUT 39 to TX OUT 32 | 7: 0 | TXSIGN [39] to TXSIGN [32] |                                                                              |

## SWITCH CORE

The ADN4605 switch core is a fully nonblocking  $40 \times 40$  array that allows multicast and broadcast configurations. The configuration of the switch core is programmed through either the serial or parallel control interface. The crosspoint configuration map, which controls the connectivity of the switch core, consists of a double rank register architecture, as shown in Figure 42.

The second rank registers contain the current state of the crosspoint. The first rank registers contain the next state. Each entry in the connection map stores six bits per output, which indicates which of the 40 inputs are connected to a given output. An entire connectivity matrix can be programmed at once by passing data from the first rank registers into the second rank by writing 0x01 to the XPT Update register (Address 0x01). An external UPDATE pin can also be used to control the data transfer as shown in Table 9.

The first rank registers store connection configurations for the crosspoint. Map 0 is the default map and is located at Address 0x04 to Address 0x2B. By default, Map 0 contains a diagonal connection configuration whereby Input 0 is connected to Output 0, Input 1 to Output 1, Input 2 to Output 2, and so on.

Similarly, by default, Map 1 contains the opposite diagonal connection configuration where Input 0 is connected to Output 39, Input 1 to Output 38, and so on. Both maps are read/write accessible registers. The active map is selected by writing to the XPT Map Table Select register (Address 0x02).

The crosspoint is configured by addressing the register assigned to the desired output and writing the desired connection data into the first rank of latches in either Map 0 or Map 1. The connection data is equivalent to the binary coded value of the input number. This process is repeated until each of the desired connections is programmed.

In situations where multiple outputs are to be programmed to a single input, a broadcast command is available. A broadcast command is issued by writing the binary value of the desired input to the XPT Broadcast register (Address 0x03). The broadcast is applied to the selected map table.

The current state of the crosspoint connectivity is available by reading the XPT Status registers (Address 0x54 to Address 0x7B). Register descriptions for Map 0, Map 1, and XPT status registers are shown in Table 12.

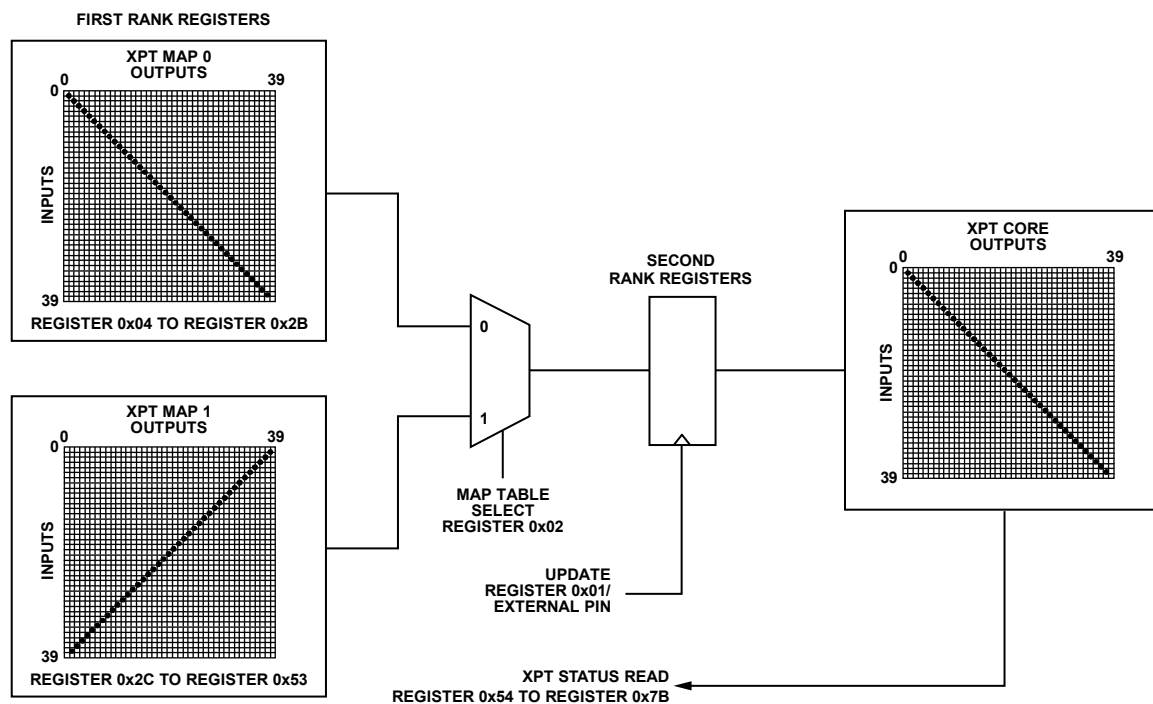


Figure 42. Crosspoint Connection Map Block Diagram

09796-009

Table 12. XPT Control Registers

| Register Address | Default              | Register Name                         | Bits | Bit Name         | Functionality Description                                        |
|------------------|----------------------|---------------------------------------|------|------------------|------------------------------------------------------------------|
| 0x00             | 0x00<br>(Write only) | Software Reset                        | 0    | Software reset   | Reset the ADN4605 registers to default values                    |
| 0x01             | 0x00<br>(Write only) | XPT Update                            | 0    | XPT Update       | Updates XPT switch core (active high)                            |
| 0x02             | 0x00                 | XPT Map Table Select                  | 0    | Map Table Select | 0: Map 0 is selected (default)<br>1: Map 1 is selected           |
| 0x03             | 0x00<br>(Write only) | XPT Broadcast                         | 5:0  | XPT BCAST [5:0]  | Assigns all output values at once for the selected XPT table map |
| 0x04 to 0x2B     | 0x00 to 0x27         | XPT Map 0<br>Control 0 to Control 39  | 5:0  | OUT x [5:0]      | Output (x = 0 to 39) connection assignments                      |
| 0x2C to 0x53     | 0x27 to 0x00         | XPT Map 1<br>Control 39 to Control 0  | 5:0  | OUT x [5:0]      | Output (x = 39 to 0) connection assignments                      |
| 0x54 to 0x7B     | 0x00 to 0x00         | XPT Status<br>Control 39 to Control 0 | 5:0  | OUT x [5:0]      | Output (x = 0 to 39) connection status                           |

## RESET

On initial power-up, or at any point in operation, the ADN4605 register set can be restored to the default values by pulling the  $\overline{\text{RESET}}$  pin low according to the control logic timing specifications. During normal operation, however, the  $\overline{\text{RESET}}$  pin must be pulled up to  $\text{DV}_{\text{CC}}$ . A software reset is also available by writing the value 0x01 to the Reset register at Address 0x00. This register is write-only.



Table 14. Transmitter Output Enable State Settings

| Register Address | Default              | Register Name                    | Bits                     | Bit Name                                         | Functionality Description                                                      |
|------------------|----------------------|----------------------------------|--------------------------|--------------------------------------------------|--------------------------------------------------------------------------------|
| 0xB0             | 0x00                 | Tx Drive Control<br>Tx3 to Tx0   | 7:6<br>5:4<br>3:2<br>1:0 | TXEN [3]<br>TXEN [2]<br>TXEN [1]<br>TXEN [0]     | 11: enabled<br>10: Tx standby<br>01: Tx squelched<br>00: Tx disabled (default) |
| 0xB1             | 0x00                 | Tx Drive Control<br>Tx7 to Tx4   | 7:6<br>5:4<br>3:2<br>1:0 | TXEN [7]<br>TXEN [6]<br>TXEN [5]<br>TXEN [4]     |                                                                                |
| 0xB2             | 0x00                 | Tx Drive Control<br>Tx11 to Tx8  | 7:6<br>5:4<br>3:2<br>1:0 | TXEN [11]<br>TXEN [10]<br>TXEN [9]<br>TXEN [8]   |                                                                                |
| 0xB3             | 0x00                 | Tx Drive Control<br>Tx15 to Tx12 | 7:6<br>5:4<br>3:2<br>1:0 | TXEN [15]<br>TXEN [14]<br>TXEN [13]<br>TXEN [12] |                                                                                |
| 0xB4             | 0x00                 | Tx Drive Control<br>Tx19 to Tx16 | 7:6<br>5:4<br>3:2<br>1:0 | TXEN [19]<br>TXEN [18]<br>TXEN [17]<br>TXEN [16] |                                                                                |
| 0xB5             | 0x00                 | Tx Drive Control<br>Tx23 to Tx20 | 7:6<br>5:4<br>3:2<br>1:0 | TXEN [23]<br>TXEN [22]<br>TXEN [21]<br>TXEN [20] |                                                                                |
| 0xB6             | 0x00                 | Tx Drive Control<br>Tx27 to Tx24 | 7:6<br>5:4<br>3:2<br>1:0 | TXEN [27]<br>TXEN [26]<br>TXEN [25]<br>TXEN [24] |                                                                                |
| 0xB7             | 0x00                 | Tx Drive Control<br>Tx31 to Tx28 | 7:6<br>5:4<br>3:2<br>1:0 | TXEN [31]<br>TXEN [30]<br>TXEN [29]<br>TXEN [28] |                                                                                |
| 0xB8             | 0x00                 | Drive Control<br>Tx35 to Tx32    | 7:6<br>5:4<br>3:2<br>1:0 | TXEN [35]<br>TXEN [34]<br>TXEN [33]<br>TXEN [32] |                                                                                |
| 0xB9             | 0x00                 | Drive Control<br>Tx39 to Tx36    | 7:6<br>5:4<br>3:2<br>1:0 | TXEN [39]<br>TXEN [38]<br>TXEN [37]<br>TXEN [36] |                                                                                |
| 0xBA             | 0x00<br>(Write only) | Tx Drive Control                 | 1:0                      | TXENBC [39]                                      |                                                                                |

The amount of high frequency boost provided by the transmitter is determined by both the output and preemphasis level settings. Table 15 provides an example of how the absolute output and preemphasis level settings determine the amount of high frequency boost at the Tx output. Note that the OLEV setting refers to the main tap output current and the PE setting refers to the delayed tap current.

The preemphasis boost equation follows:

$$Gain[dB] = 20 \times \log_{10} \left( 1 + \frac{V_{SW-PE} - V_{SW-DC}}{V_{SW-DC}} \right) \quad (1)$$

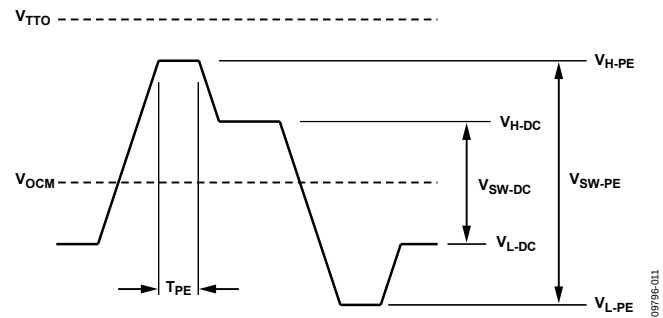


Figure 44. Signal Level Definitions

Table 15. Preemphasis Boost and Overshoot vs. Setting Example

| PE Setting | Delayed Tap Current (mA) | OLEV Setting | Main Tap Current (mA) | Gain (dB) | Overshoot (%) | DC Swing (mV p-p Diff) |
|------------|--------------------------|--------------|-----------------------|-----------|---------------|------------------------|
| 0          | 0                        | 4            | 16                    | 0.00      | 0.00          | 800                    |
| 3          | 4                        | 5            | 20                    | 3.52      | 50.00         | 800                    |
| 7          | 8                        | 6            | 24                    | 6.02      | 100.00        | 800                    |
| 7          | 8                        | 4            | 16                    | 9.54      | 200.00        | 400                    |
| 7          | 8                        | 3            | 12                    | 13.98     | 400.00        | 200                    |

Table 16. Symbol Definitions

| Symbol                       | Formula                                              | Definition                                                           |
|------------------------------|------------------------------------------------------|----------------------------------------------------------------------|
| $I_{DC}$                     | Programmable                                         | Output current for main tap output level (OLEV)                      |
| $I_{PE}$                     | Programmable                                         | Output current for PE delayed tap (PE)                               |
| $I_{TTO}$                    | $I_{DC} + I_{PE}$                                    | Total transmitter output current                                     |
| $V_{DPP-DC}$                 | $25 \Omega \times I_{DC} \times 2$                   | Peak-to-peak differential voltage swing of nonpreemphasized waveform |
| $V_{DPP-PE}$                 | $25 \Omega \times I_{TTO} \times 2$                  | Peak-to-peak differential voltage swing of preemphasized waveform    |
| $V_{SW-DC}$                  | $V_{DPP-DC}/2 = V_{H-DC} - V_{L-DC}$                 | DC single-ended voltage swing                                        |
| $V_{SW-PE}$                  | $V_{DPP-PE}/2 = V_{H-PE} - V_{L-PE}$                 | Preemphasized single-ended voltage swing                             |
| $\Delta V_{OCM\_DC-COUPLED}$ | $25 \Omega \times I_{TTO}/2$                         | Output common-mode shift, dc-coupled outputs                         |
| $\Delta V_{OCM\_AC-COUPLED}$ | $50 \Omega \times I_{TTO}/2$                         | Output common-mode shift, ac-coupled outputs                         |
| $V_{OCM}$                    | $V_{TTO} - \Delta V_{OCM} = (V_{H-DC} + V_{L-DC})/2$ | Output common-mode voltage                                           |
| $V_{H-DC}$                   | $V_{TTO} - \Delta V_{OCM} + V_{DPP-DC}/2$            | DC single-ended output high voltage                                  |
| $V_{L-DC}$                   | $V_{TTO} - \Delta V_{OCM} - V_{DPP-DC}/2$            | DC single-ended output low voltage                                   |
| $V_{H-PE}$                   | $V_{TTO} - \Delta V_{OCM} + V_{DPP-PE}/2$            | Maximum single-ended output voltage                                  |
| $V_{L-PE}$                   | $V_{TTO} - \Delta V_{OCM} - V_{DPP-PE}/2$            | Minimum single-ended output voltage                                  |

## TERMINATION

The inputs and outputs include integrated 50  $\Omega$  termination resistors. The internal resistors can be disabled for applications that require external termination resistors. For example, disabling the integrated 50  $\Omega$  termination resistors allow alternative termination values such as 75  $\Omega$  as shown in Figure 45.

Note that the integrated 50  $\Omega$  termination resistors are optimal for high data rate digital signaling. Disabling the terminations can reduce the overall performance.

The termination control for the receiver inputs can be accessed through Register Address 0xD0 (Input 0 to Input 19) and

Register Address 0xD1 (Input 20 to Input 39). The termination control for the transmitter outputs can be accessed through Register Address 0xBC (Output 0 to Output 19) and Register Address 0xBD (Output 20 to Output 39).

Table 17 shows the termination control registers. Each bit controls the terminations settings for four inputs/outputs. A Logic 0 enables the terminations for the respective group. A Logic 1 disables the terminations for the respective group. The terminations are enabled by default.

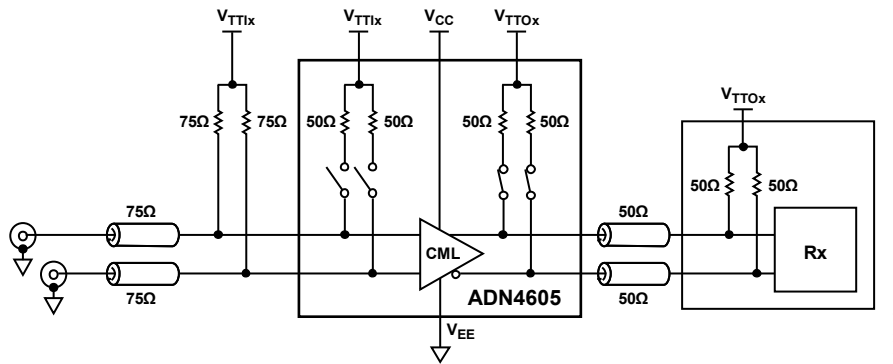


Figure 45. 75  $\Omega$  to 50  $\Omega$  Impedance Translator

Table 17. Termination Control Registers

| Register Address | Default | Register Name          | Bit | Bit Name | Description                                 | Functionality                                         |
|------------------|---------|------------------------|-----|----------|---------------------------------------------|-------------------------------------------------------|
| 0xBD             | 0x00    | Tx Termination Control | 4   | TXB_TERM | Output [39:36] (B side) termination control | 0 = terminations enabled<br>1 = terminations disabled |
|                  |         |                        | 3   | TXB_TERM | Output [35:32] (B side) termination control |                                                       |
|                  |         |                        | 2   | TXB_TERM | Output [31:28] (B side) termination control |                                                       |
|                  |         |                        | 1   | TXB_TERM | Output [27:24] (B side) termination control |                                                       |
|                  |         |                        | 0   | TXB_TERM | Output [23:20] (B side) termination control |                                                       |
| 0xBC             | 0x00    | Tx Termination Control | 4   | TXA_TERM | Output [19:16] (A side) termination control |                                                       |
|                  |         |                        | 3   | TXA_TERM | Output [15:12] (A side) termination control |                                                       |
|                  |         |                        | 2   | TXA_TERM | Output [11:8] (A side) termination control  |                                                       |
|                  |         |                        | 1   | TXA_TERM | Output [7:4] (A side) termination control   |                                                       |
|                  |         |                        | 0   | TXA_TERM | Output [3:0] (A side) termination control   |                                                       |
| 0xD1             | 0x00    | Rx Termination Control | 4   | RXB_TERM | Input [39:36] (B side) termination control  |                                                       |
|                  |         |                        | 3   | RXB_TERM | Input [35:32] (B side) termination control  |                                                       |
|                  |         |                        | 2   | RXB_TERM | Input [31:28] (B side) termination control  |                                                       |
|                  |         |                        | 1   | RXB_TERM | Input [27:24] (B side) termination control  |                                                       |
|                  |         |                        | 0   | RXB_TERM | Input [23:20] (B side) termination control  |                                                       |
| 0xD0             | 0x00    | Rx Termination Control | 4   | RXA_TERM | Input [19:16] (A side) termination control  |                                                       |
|                  |         |                        | 3   | RXA_TERM | Input [15:12] (A side) termination control  |                                                       |
|                  |         |                        | 2   | RXA_TERM | Input [11:8] (A side) termination control   |                                                       |
|                  |         |                        | 1   | RXA_TERM | Input [7:4] (A side) termination control    |                                                       |
|                  |         |                        | 0   | RXA_TERM | Input [3:0] (A side) termination control    |                                                       |

## I<sup>2</sup>C SERIAL CONTROL INTERFACE

The ADN4605 register set is controlled through a 2-wire I<sup>2</sup>C interface. To access the I<sup>2</sup>C serial interface, both the SER/PAR line and I<sup>2</sup>C/SPI lines must be held at logic high. The ADN4605 acts only as an I<sup>2</sup>C slave device. Therefore, the I<sup>2</sup>C bus in the system needs to include an I<sup>2</sup>C master to configure the ADN4605 and other I<sup>2</sup>C devices that may be on the bus.

The ADN4605 I<sup>2</sup>C interface can be run in the standard (100 kHz) and fast (400 kHz) modes. The SDA line only changes value when the SCL pin is low with two exceptions. To indicate the beginning or continuation of a transfer, the SDA pin is driven low while the SCL pin is high; to indicate the end of a transfer, the SDA line is driven high while the SCL line is high. Therefore, it is important to control the SCL clock to toggle only when the SDA line is stable unless indicating a start, repeated start, or stop condition. To establish I<sup>2</sup>C communication with the ADN4605, parallel address lines (ADDR[7:1]) need to be configured to the user-assigned I<sup>2</sup>C device address as shown in Table 18.

**Table 18. Example of I<sup>2</sup>C Device Address Assignment**

| A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 | I <sup>2</sup> C Device Address |
|----|----|----|----|----|----|----|----|---------------------------------|
| 1  | 0  | 0  | 1  | 0  | 0  | 0  | X  | 0x90                            |
| 1  | 0  | 0  | 1  | 0  | 0  | 1  | X  | 0x92                            |
| 1  | 0  | 0  | 1  | 0  | 1  | 0  | X  | 0x94                            |
| 1  | 0  | 0  | 1  | 0  | 1  | 1  | X  | 0x96                            |

### I<sup>2</sup>C DATA WRITE

To write data to the ADN4605 register set, a microcontroller, or any other I<sup>2</sup>C master, must send the appropriate control signals to the ADN4605 slave device. The steps to be followed are listed below; the signals are controlled by the I<sup>2</sup>C master unless otherwise specified. A diagram of the procedure is shown in Figure 46.

1. Send a start condition (while holding the SCL line high, pull the SDA line low).

2. Send the ADN4605 part address (seven bits) whose bits are controlled by the input pins ADDR[7:1]. This transfer should be MSB first.
3. Send the write indicator bit (0).
4. Wait for the ADN4605 to acknowledge the request.
5. Send the register address (eight bits) to which data is to be written. This transfer should be MSB first.
6. Wait for the ADN4605 to acknowledge the request.
7. Send the data (eight bits) to be written to the register whose address was set in Step 5. This transfer should be MSB first.
8. Wait for the ADN4605 to acknowledge the request.
9. Do one or more of the following:
  - a. Send a stop condition (while holding the SCL line high, pull the SDA line high) and release control of the bus.
  - b. Send a repeated start condition (while holding the SCL line high, pull the SDA line low) and continue with Step 2 of the write procedure (see the I<sup>2</sup>C Timing Specifications section) to perform a write.
  - c. Send a repeated start condition (while holding the SCL line high, pull the SDA line low) and continue with Step 2 of this procedure to perform a read from another address.
  - d. Send a repeated start condition (while holding the SCL line high, pull the SDA line low) and continue with Step 8 of this procedure to perform a read from the same address.

The ADN4605 write process is shown in Figure 46. The SCL signal is shown along with a general write operation and a specific example. In the example, Data 0x4B is written to Address 0x6D of an ADN4605 part with a part address of 0x92. The ADN4605 device address selections are more flexible than shown. It is important to note that the SDA line only changes when the SCL line is low, except for the case of sending a start, stop, or repeated start condition, Step 1 and Step 9 in this case.

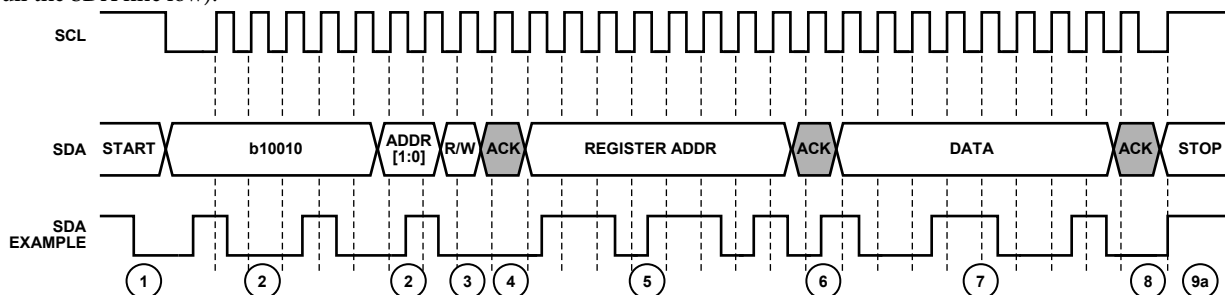


Figure 46. I<sup>2</sup>C Write Diagram

## I<sup>2</sup>C DATA READ

To read data from the ADN4605 register set, a microcontroller, or any other I<sup>2</sup>C master needs to send the appropriate control signals to the ADN4605 slave device. The steps are listed below; the signals are controlled by the I<sup>2</sup>C master unless otherwise specified. A diagram of the procedure is shown in Figure 47.

1. Send a start condition (while holding the SCL line high, pull the SDA line low).
2. Send the ADN4605 part address (seven bits) whose bits are controlled by the input pins ADDR[7:1]. This transfer should be MSB first.
3. Send the write indicator bit (0).
4. Wait for the ADN4605 to acknowledge the request.
5. Send the register address (eight bits) from which data is to be read. This transfer should be MSB first. The register address is kept in memory in the ADN4605 until the part is reset or the register address is written over with the same procedure (Step 1 to Step 6).
6. Wait for the ADN4605 to acknowledge the request.
7. Send a repeated start condition (while holding the SCL line high, pull the SDA line low).
8. Send the ADN4605 part address (seven bits) whose bits are controlled by the input pins ADDR[7:1]. This transfer should be MSB first.
9. Send the read indicator bit (1).
10. Wait for the ADN4605 to acknowledge the request.
11. The ADN4605 then serially transfers the data (eight bits) held in the register indicated by the address set in Step 5.

12. Acknowledge the data.

13. Do one or more of the following:

- a. Send a stop condition (while holding the SCL line high pull the SDA line high) and release control of the bus.
- b. Send a repeated start condition (while holding the SCL line high, pull the SDA line low) and continue with Step 2 of the write procedure (see the I<sup>2</sup>C Data Write section) to perform a write.
- c. Send a repeated start condition (while holding the SCL line high, pull the SDA line low) and continue with Step 2 of this procedure to perform a read from another address.
- d. Send a repeated start condition (while holding the SCL line high, pull the SDA line low) and continue with Step 8 of this procedure to perform a read from the same address.

The ADN4605 read process is shown in Figure 47. The SCL signal is shown along with a general read operation and a specific example. In the example, Data 0x49 is read from Address 0x6D of an ADN4605 part with a part address of 0x92. The part address is seven bits wide and is composed of the ADN4605 (ADDR[7:1]). In this example, the ADDR[1:0] bits are set to b01.

In Figure 47, the corresponding step number is visible in the circle under the waveform. The SCL line is driven by the I<sup>2</sup>C master and never by the ADN4605 slave. As for the SDA line, the data in the shaded polygons is driven by the ADN4605, whereas the data in the nonshaded polygons is driven by the I<sup>2</sup>C master. The end phase case shown is that of Step 13a.

Note that the SDA line only changes when the SCL line is low, except for the case of sending a start, stop, or repeated start condition, as in Step 1, Step 7, and Step 13. In Figure 47, A is the same as ACK. Equally, Sr represents a repeated start where the SDA line is brought high before SCL is raised. SDA is then dropped while SCL is still high.

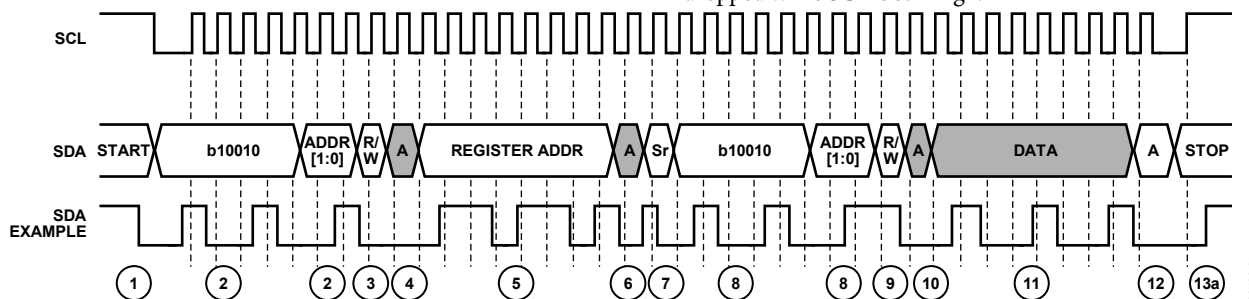


Figure 47. I<sup>2</sup>C Read Diagram

## SPI SERIAL CONTROL INTERFACE

The SPI serial interface of the ADN4605 consists of four wires:  $\overline{\text{CS}}$ , SCK, SDI, and SDO. In order to access the SPI interface the SER/ $\overline{\text{PAR}}$  line must be held at logic high and the I<sup>2</sup>C/ $\overline{\text{SPI}}$  line must be held at logic low. The  $\overline{\text{CS}}$  pin is used to select the device when more than one device is connected to the serial clock and data lines and must be held at logic low to enable write/read capability to the device when in SPI control mode.

The SCK is used to clock data in and out of the part. The SDI line is used to write to the registers, and the SDO line is used to read data back from the registers. Data on SDI line is clocked on the rising edge of SCK. Data on SDO changes on the falling edge of SCK. The recommended pull-up resistor value is between 500  $\Omega$  and 1 k $\Omega$ . Strong pull-ups are needed when serial clock speeds that are close to the maximum limit are used or when the SPI interface lines are experiencing large capacitive loading. Larger resistor values can be used for pull-up resistors when the serial clock speed is reduced.

The part operates in a slave mode and requires an externally applied serial clock to the SCK input. The serial interface is designed to allow the part to be interfaced to systems that provide a serial clock that is synchronized to the serial data.

There are two types of serial operations, a read and a write. Command words are used to distinguish between a read and a write operation as shown in Table 19.

**Table 19. SPI Command Words**

|               |                  |
|---------------|------------------|
| Write Command | 0x02 (0000 0010) |
| Read Command  | 0x03 (0000 0011) |

### Write Operation

Figure 48 shows the diagram for a write operation to the ADN4605. Data is clocked into the registers on the rising edge of SCK. When the  $\overline{\text{CS}}$  line is high, the SDI and SDO lines are in three-state mode. Only when the  $\overline{\text{CS}}$  goes from a high to a low does the part accept any data on the SDI line. The 8-bit write command must precede the register address byte. The register address byte is then followed by the data byte as shown in Figure 48.

To allow continuous writes, the address pointer register auto-increments by one without having to load the address pointer register each time. Subsequent data bytes are written into sequential registers. Note that not all registers in the 256-byte address space exist and not all registers are writable. Zeroes should be entered for nonexistent address fields when implementing a continuous write operation. Address space 0xE0 to Address 0xFF is reserved and should not be overwritten.

### Read Operation

To read back from a register, first send the read command followed by the desired register address. Subsequent clock cycles, with  $\overline{\text{CS}}$  asserted low, stream data starting from the desired register address onto SDO, MSB first. SDO changes on the falling edge of SCK. Multiple data reads are possible in SPI interface mode because the address pointer register is auto-incremented.

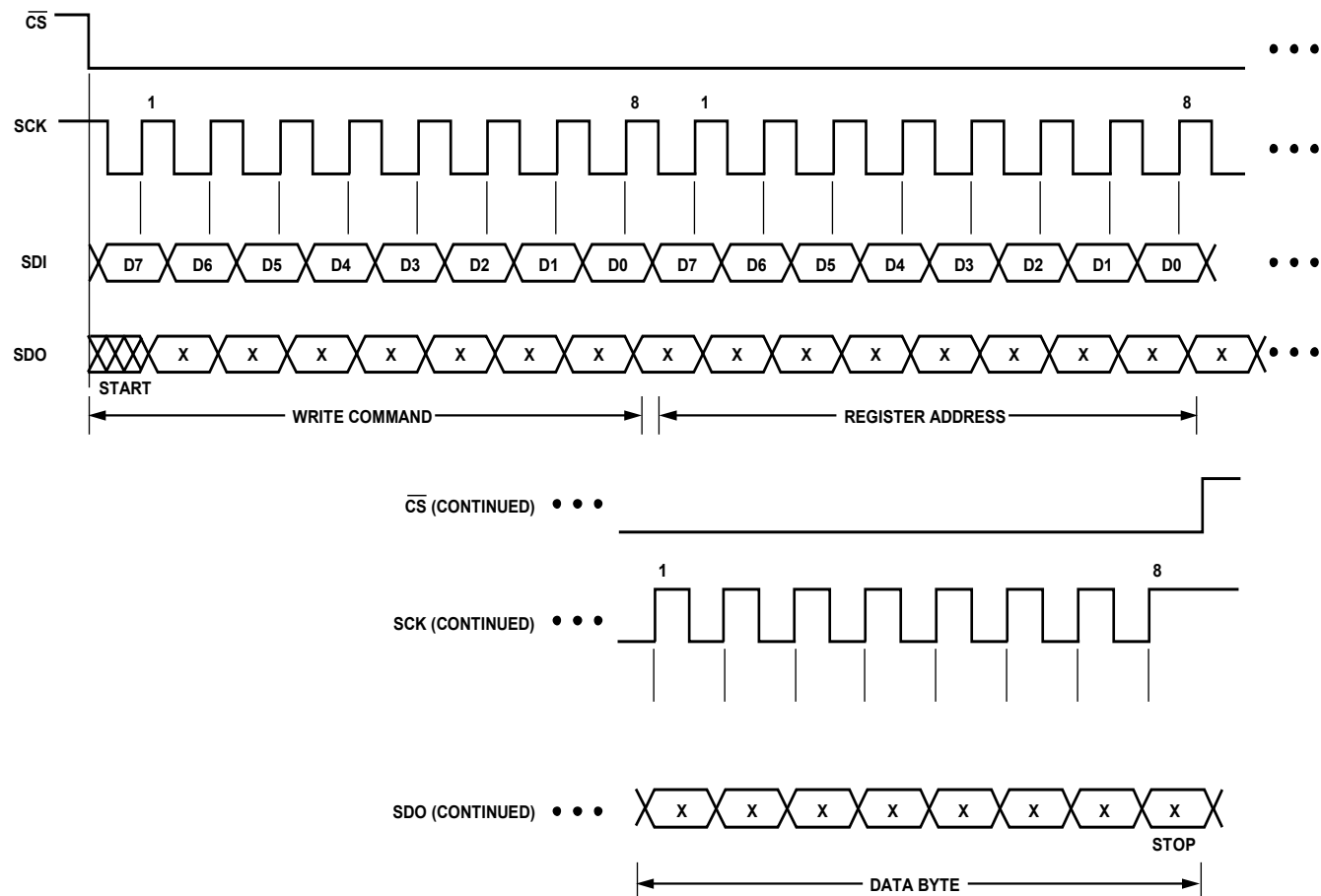


Figure 48. SPI-Writing to the Address Pointer Register Followed by a Single Byte of Data to the Selected Register

09756-015

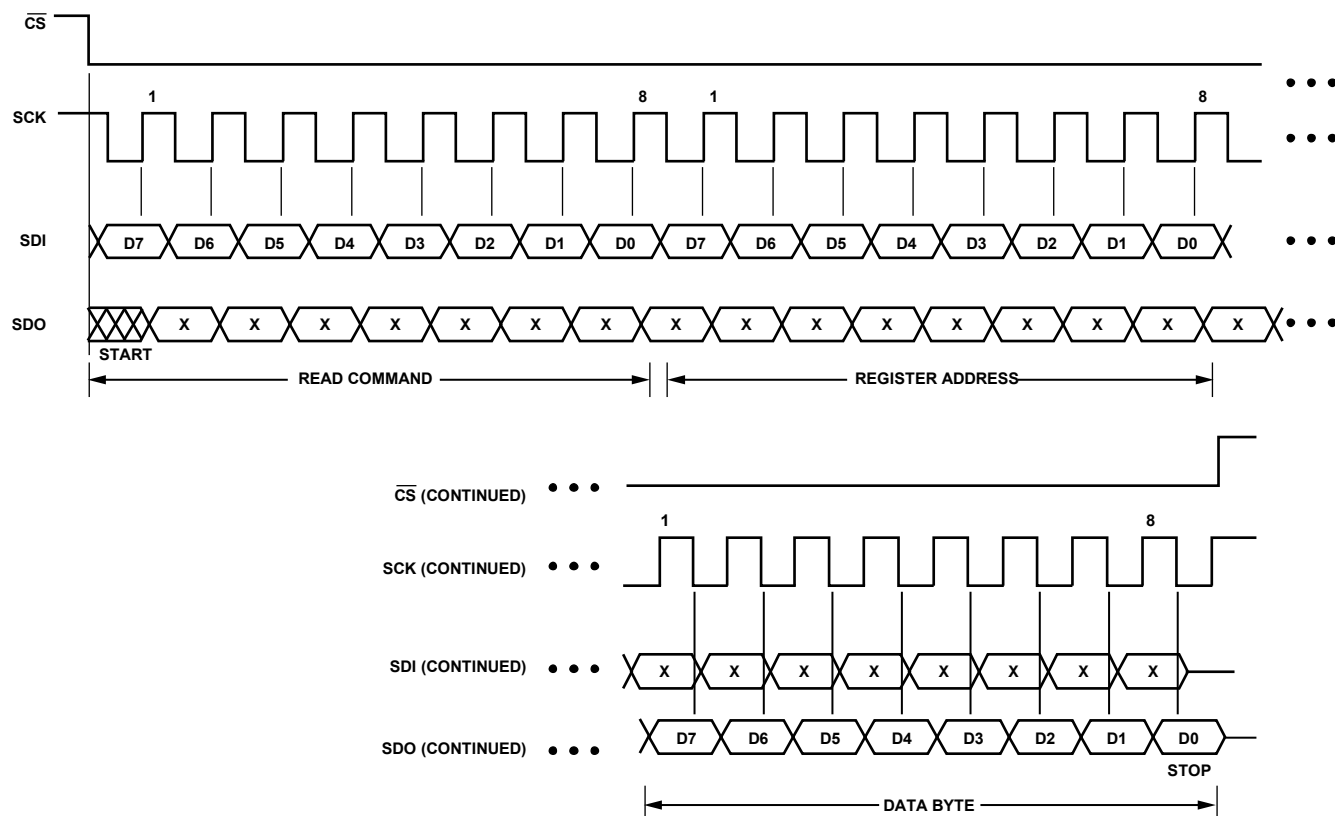


Figure 49. SPI—Reading a Single Byte of Data from a Selected Register

007956-016

## PARALLEL CONTROL INTERFACE

The parallel control interface of the ADN4605 consists of nineteen wires: ADDR[7:0], DATA[7:0],  $\overline{\text{WE}}$ ,  $\overline{\text{RE}}$ , and  $\overline{\text{CS}}$ . To access the parallel control interface, the SER/PAR line must be held at logic low. The  $\overline{\text{CS}}$  line is used to select a device when one or more devices share the same address and data lines. The  $\overline{\text{CS}}$  line must be held at logic low to enable write/read capability to the device when in parallel control mode.

### ADDRESS INPUTS: ADDR[7:0]

The binary coded address applied to the address lines determines which device registers are being programmed or read back.

### DATA INPUTS/OUTPUTS: DATA[7:0]

In write mode, the binary encoded data applied to the data lines (DATA[7:0]) determine the configuration setting of the register specified by the address lines (ADDR[7:0]).

In read mode, data lines (DATA[7:0]) are low impedance outputs indicating the data byte stored in the register specified by the address lines (ADDR[7:0]). Note that some registers are write only and may not be read from (see Table 20). The read-back drivers are designed to drive high impedances only ( $>1 \text{ k}\Omega$ ).

## WRITE OPERATION

For first rank write enable, forcing this pin to logic low allows the data on the DATA[7:0] lines to be stored in the first rank latch for the register specified by the address lines (ADDR[7:0]). The data is latched during the high-to-low transition of the write enable pulse. The  $\overline{\text{WE}}$  line must be returned to a logic high state after the write cycle to avoid overwriting the first rank data.

## READ OPERATION

For second rank read enable, forcing this line to a logic low state enables the output drivers on the bidirectional data lines (DATA[7:0]), placing the logic in readback mode of operation. The register selected to read from is determined by the binary encoded data configured on the address lines (ADDR[7:0]). When the read enable line is at a logic low, the data stored in the specified register will be latched onto the data lines (DATA[7:0]). The  $\overline{\text{RE}}$  line is higher priority than the  $\overline{\text{WE}}$  line; therefore, first rank programming is not possible while in readback mode. Note that some registers are defined as write only and are not accessible in readback mode (see Table 20).

## REGISTER MAP

In the Register Map, when settings are provided in the Description column for the first bit, note that these settings apply to all bits with the same function.

**Table 20. Register Map**

| Address: Channel | Default            | Register Name        | Bits | Bit Name         | Description                                  |
|------------------|--------------------|----------------------|------|------------------|----------------------------------------------|
| 0x00             | 0x00<br>Write only | Software Reset       | 0    | Reset            | Software reset                               |
| 0x01             | 0x0<br>Write only  | XPT Update           | 0    | XPT Update       | Updates crosspoint switch core               |
| 0x02             | 0x00               | XPT Map Table Select | 0    | Map Table Select | 0: Map 0 is selected<br>1: Map 1 is selected |
| 0x03             | Write only         | XPT Broadcast        | 5:0  | XPT BCAST [5:0]  | All outputs connection assignment            |
| 0x04             | 0x00               | XPT Map 0 Control 0  | 5:0  | OUT 0 [5:0]      | Output 0 connection assignment               |
| 0x05             | 0x01               | XPT Map 0 Control 1  | 5:0  | OUT 1 [5:0]      | Output 1 connection assignment               |
| 0x06             | 0x02               | XPT Map 0 Control 2  | 5:0  | OUT 2 [5:0]      | Output 2 connection assignment               |
| 0x07             | 0x03               | XPT Map 0 Control 3  | 5:0  | OUT 3 [5:0]      | Output 3 connection assignment               |
| 0x08             | 0x04               | XPT Map 0 Control 4  | 5:0  | OUT 4 [5:0]      | Output 4 connection assignment               |
| 0x09             | 0x05               | XPT Map 0 Control 5  | 5:0  | OUT 5 [5:0]      | Output 5 connection assignment               |
| 0x0A             | 0x06               | XPT Map 0 Control 6  | 5:0  | OUT 6 [5:0]      | Output 6 connection assignment               |
| 0x0B             | 0x07               | XPT Map 0 Control 7  | 5:0  | OUT 7 [5:0]      | Output 7 connection assignment               |
| 0x0C             | 0x08               | XPT Map 0 Control 8  | 5:0  | OUT 8 [5:0]      | Output 8 connection assignment               |
| 0x0D             | 0x09               | XPT Map 0 Control 9  | 5:0  | OUT 9 [5:0]      | Output 9 connection assignment               |
| 0x0E             | 0x0A               | XPT Map 0 Control 10 | 5:0  | OUT 10 [5:0]     | Output 10 connection assignment              |
| 0x0F             | 0x0B               | XPT Map 0 Control 11 | 5:0  | OUT 11 [5:0]     | Output 11 connection assignment              |
| 0x10             | 0x0C               | XPT Map 0 Control 12 | 5:0  | OUT 12 [5:0]     | Output 12 connection assignment              |
| 0x11             | 0x0D               | XPT Map 0 Control 13 | 5:0  | OUT 13 [5:0]     | Output 13 connection assignment              |
| 0x12             | 0x0E               | XPT Map 0 Control 14 | 5:0  | OUT 14 [5:0]     | Output 14 connection assignment              |
| 0x13             | 0x0F               | XPT Map 0 Control 15 | 5:0  | OUT 15 [5:0]     | Output 15 connection assignment              |
| 0x14             | 0x10               | XPT Map 0 Control 16 | 5:0  | OUT 16 [5:0]     | Output 16 connection assignment              |
| 0x15             | 0x11               | XPT Map 0 Control 17 | 5:0  | OUT 17 [5:0]     | Output 17 connection assignment              |
| 0x16             | 0x12               | XPT Map 0 Control 18 | 5:0  | OUT 18 [5:0]     | Output 18 connection assignment              |
| 0x17             | 0x13               | XPT Map 0 Control 19 | 5:0  | OUT 19 [5:0]     | Output 19 connection assignment              |
| 0x18             | 0x14               | XPT Map 0 Control 20 | 5:0  | OUT 20 [5:0]     | Output 20 connection assignment              |
| 0x19             | 0x15               | XPT Map 0 Control 21 | 5:0  | OUT 21 [5:0]     | Output 21 connection assignment              |
| 0x1A             | 0x16               | XPT Map 0 Control 22 | 5:0  | OUT 22 [5:0]     | Output 22 connection assignment              |
| 0x1B             | 0x17               | XPT Map 0 Control 23 | 5:0  | OUT 23 [5:0]     | Output 23 connection assignment              |
| 0x1C             | 0x18               | XPT Map 0 Control 24 | 5:0  | OUT 24 [5:0]     | Output 24 connection assignment              |
| 0x1D             | 0x19               | XPT Map 0 Control 25 | 5:0  | OUT 25 [5:0]     | Output 25 connection assignment              |
| 0x1E             | 0x1A               | XPT Map 0 Control 26 | 5:0  | OUT 26 [5:0]     | Output 26 connection assignment              |
| 0x1F             | 0x1B               | XPT Map 0 Control 27 | 5:0  | OUT 27 [5:0]     | Output 27 connection assignment              |
| 0x20             | 0x1C               | XPT Map 0 Control 28 | 5:0  | OUT 28 [5:0]     | Output 28 connection assignment              |
| 0x21             | 0x1D               | XPT Map 0 Control 29 | 5:0  | OUT 29 [5:0]     | Output 29 connection assignment              |
| 0x22             | 0x1E               | XPT Map 0 Control 30 | 5:0  | OUT 30 [5:0]     | Output 30 connection assignment              |
| 0x23             | 0x1F               | XPT Map 0 Control 31 | 5:0  | OUT 31 [5:0]     | Output 31 connection assignment              |
| 0x24             | 0x20               | XPT Map 0 Control 32 | 5:0  | OUT 32 [5:0]     | Output 32 connection assignment              |
| 0x25             | 0x21               | XPT Map 0 Control 33 | 5:0  | OUT 33 [5:0]     | Output 33 connection assignment              |
| 0x26             | 0x22               | XPT Map 0 Control 34 | 5:0  | OUT 34 [5:0]     | Output 34 connection assignment              |
| 0x27             | 0x23               | XPT Map 0 Control 35 | 5:0  | OUT 35 [5:0]     | Output 35 connection assignment              |
| 0x28             | 0x24               | XPT Map 0 Control 36 | 5:0  | OUT 36 [5:0]     | Output 36 connection assignment              |
| 0x29             | 0x25               | XPT Map 0 Control 37 | 5:0  | OUT 37 [5:0]     | Output 37 connection assignment              |
| 0x2A             | 0x26               | XPT Map 0 Control 38 | 5:0  | OUT 38 [5:0]     | Output 38 connection assignment              |
| 0x2B             | 0x27               | XPT Map 0 Control 39 | 5:0  | OUT 39 [5:0]     | Output 39 connection assignment              |

| Address: Channel | Default | Register Name        | Bits | Bit Name     | Description                     |
|------------------|---------|----------------------|------|--------------|---------------------------------|
| 0x2C             | 0x27    | XPT Map 1 Control 0  | 5:0  | OUT 0 [5:0]  | Output 0 connection assignment  |
| 0x2D             | 0x26    | XPT Map 1 Control 1  | 5:0  | OUT 1 [5:0]  | Output 1 connection assignment  |
| 0x2E             | 0x25    | XPT Map 1 Control 2  | 5:0  | OUT 2 [5:0]  | Output 2 connection assignment  |
| 0x2F             | 0x24    | XPT Map 1 Control 3  | 5:0  | OUT 3 [5:0]  | Output 3 connection assignment  |
| 0x30             | 0x23    | XPT Map 1 Control 4  | 5:0  | OUT 4 [5:0]  | Output 4 connection assignment  |
| 0x31             | 0x22    | XPT Map 1 Control 5  | 5:0  | OUT 5 [5:0]  | Output 5 connection assignment  |
| 0x32             | 0x21    | XPT Map 1 Control 6  | 5:0  | OUT 6 [5:0]  | Output 6 connection assignment  |
| 0x33             | 0x20    | XPT Map 1 Control 7  | 5:0  | OUT 7 [5:0]  | Output 7 connection assignment  |
| 0x34             | 0x1F    | XPT Map 1 Control 8  | 5:0  | OUT 8 [5:0]  | Output 8 connection assignment  |
| 0x35             | 0x1E    | XPT Map 1 Control 9  | 5:0  | OUT 9 [5:0]  | Output 9 connection assignment  |
| 0x36             | 0x1D    | XPT Map 1 Control 10 | 5:0  | OUT 10 [5:0] | Output 10 connection assignment |
| 0x37             | 0x1C    | XPT Map 1 Control 11 | 5:0  | OUT 11 [5:0] | Output 11 connection assignment |
| 0x38             | 0x1B    | XPT Map 1 Control 12 | 5:0  | OUT 12 [5:0] | Output 12 connection assignment |
| 0x39             | 0x1A    | XPT Map 1 Control 13 | 5:0  | OUT 13 [5:0] | Output 13 connection assignment |
| 0x3A             | 0x19    | XPT Map 1 Control 14 | 5:0  | OUT 14 [5:0] | Output 14 connection assignment |
| 0x3B             | 0x18    | XPT Map 1 Control 15 | 5:0  | OUT 15 [5:0] | Output 15 connection assignment |
| 0x3C             | 0x17    | XPT Map 1 Control 16 | 5:0  | OUT 16 [5:0] | Output 16 connection assignment |
| 0x3D             | 0x16    | XPT Map 1 Control 17 | 5:0  | OUT 17 [5:0] | Output 17 connection assignment |
| 0x3E             | 0x15    | XPT Map 1 Control 18 | 5:0  | OUT 18 [5:0] | Output 18 connection assignment |
| 0x3F             | 0x14    | XPT Map 1 Control 19 | 5:0  | OUT 19 [5:0] | Output 19 connection assignment |
| 0x40             | 0x13    | XPT Map 1 Control 20 | 5:0  | OUT 20 [5:0] | Output 20 connection assignment |
| 0x41             | 0x12    | XPT Map 1 Control 21 | 5:0  | OUT 21 [5:0] | Output 21 connection assignment |
| 0x42             | 0x11    | XPT Map 1 Control 22 | 5:0  | OUT 22 [5:0] | Output 22 connection assignment |
| 0x43             | 0x10    | XPT Map 1 Control 23 | 5:0  | OUT 23 [5:0] | Output 23 connection assignment |
| 0x44             | 0x0F    | XPT Map 1 Control 24 | 5:0  | OUT 24 [5:0] | Output 24 connection assignment |
| 0x45             | 0x0E    | XPT Map 1 Control 25 | 5:0  | OUT 25 [5:0] | Output 25 connection assignment |
| 0x46             | 0x0D    | XPT Map 1 Control 26 | 5:0  | OUT 26 [5:0] | Output 26 connection assignment |
| 0x47             | 0x0C    | XPT Map 1 Control 27 | 5:0  | OUT 27 [5:0] | Output 27 connection assignment |
| 0x48             | 0x0B    | XPT Map 1 Control 28 | 5:0  | OUT 28 [5:0] | Output 28 connection assignment |
| 0x49             | 0x0A    | XPT Map 1 Control 29 | 5:0  | OUT 29 [5:0] | Output 29 connection assignment |
| 0x4A             | 0x09    | XPT Map 1 Control 30 | 5:0  | OUT 30 [5:0] | Output 30 connection assignment |
| 0x4B             | 0x08    | XPT Map 1 Control 31 | 5:0  | OUT 31 [5:0] | Output 31 connection assignment |
| 0x4C             | 0x07    | XPT Map 1 Control 32 | 5:0  | OUT 32 [5:0] | Output 32 connection assignment |
| 0x4D             | 0x06    | XPT Map 1 Control 33 | 5:0  | OUT 33 [5:0] | Output 33 connection assignment |
| 0x4E             | 0x05    | XPT Map 1 Control 34 | 5:0  | OUT 34 [5:0] | Output 34 connection assignment |
| 0x4F             | 0x04    | XPT Map 1 Control 35 | 5:0  | OUT 35 [5:0] | Output 35 connection assignment |
| 0x50             | 0x03    | XPT Map 1 Control 36 | 5:0  | OUT 36 [5:0] | Output 36 connection assignment |
| 0x51             | 0x02    | XPT Map 1 Control 37 | 5:0  | OUT 37 [5:0] | Output 37 connection assignment |
| 0x52             | 0x01    | XPT Map 1 Control 38 | 5:0  | OUT 38 [5:0] | Output 38 connection assignment |
| 0x53             | 0x00    | XPT Map 1 Control 39 | 5:0  | OUT 39 [5:0] | Output 39 connection assignment |
| 0x54             | 0x00    | XPT Status 0         | 5:0  | OUT 0 [5:0]  | Output 0 connection status      |
| 0x55             | 0x00    | XPT Status 1         | 5:0  | OUT 1 [5:0]  | Output 1 connection status      |
| 0x56             | 0x00    | XPT Status 2         | 5:0  | OUT 2 [5:0]  | Output 2 connection status      |
| 0x57             | 0x00    | XPT Status 3         | 5:0  | OUT 3 [5:0]  | Output 3 connection status      |
| 0x58             | 0x00    | XPT Status 4         | 5:0  | OUT 4 [5:0]  | Output 4 connection status      |
| 0x59             | 0x00    | XPT Status 5         | 5:0  | OUT 5 [5:0]  | Output 5 connection status      |
| 0x5A             | 0x00    | XPT Status 6         | 5:0  | OUT 6 [5:0]  | Output 6 connection status      |
| 0x5B             | 0x00    | XPT Status 7         | 5:0  | OUT 7 [5:0]  | Output 7 connection status      |
| 0x5C             | 0x00    | XPT Status 8         | 5:0  | OUT 8 [5:0]  | Output 8 connection status      |
| 0x5D             | 0x00    | XPT Status 9         | 5:0  | OUT 9 [5:0]  | Output 9 connection status      |
| 0x5E             | 0x00    | XPT Status 10        | 5:0  | OUT 10 [5:0] | Output 10 connection status     |
| 0x5F             | 0x00    | XPT Status 11        | 5:0  | OUT 11 [5:0] | Output 11 connection status     |
| 0x60             | 0x00    | XPT Status 12        | 5:0  | OUT 12 [5:0] | Output 12 connection status     |

| Address: Channel | Default | Register Name   | Bits | Bit Name     | Description                                                      |
|------------------|---------|-----------------|------|--------------|------------------------------------------------------------------|
| 0x61             | 0x00    | XPT Status 13   | 5:0  | OUT 13 [5:0] | Output 13 connection status                                      |
| 0x62             | 0x00    | XPT Status 14   | 5:0  | OUT 14 [5:0] | Output 14 connection status                                      |
| 0x63             | 0x00    | XPT Status 15   | 5:0  | OUT 15 [5:0] | Output 15 connection status                                      |
| 0x64             | 0x00    | XPT Status 16   | 5:0  | OUT 16 [5:0] | Output 16 connection status                                      |
| 0x65             | 0x00    | XPT Status 17   | 5:0  | OUT 17 [5:0] | Output 17 connection status                                      |
| 0x66             | 0x00    | XPT Status 18   | 5:0  | OUT 18 [5:0] | Output 18 connection status                                      |
| 0x67             | 0x00    | XPT Status 19   | 5:0  | OUT 19 [5:0] | Output 19 connection status                                      |
| 0x68             | 0x00    | XPT Status 20   | 5:0  | OUT 20 [5:0] | Output 20 connection status                                      |
| 0x69             | 0x00    | XPT Status 21   | 5:0  | OUT 21 [5:0] | Output 21 connection status                                      |
| 0x6A             | 0x00    | XPT Status 22   | 5:0  | OUT 22 [5:0] | Output 22 connection status                                      |
| 0x6B             | 0x00    | XPT Status 23   | 5:0  | OUT 23 [5:0] | Output 23 connection status                                      |
| 0x6C             | 0x00    | XPT Status 24   | 5:0  | OUT 24 [5:0] | Output 24 connection status                                      |
| 0x6D             | 0x00    | XPT Status 25   | 5:0  | OUT 25 [5:0] | Output 25 connection status                                      |
| 0x6E             | 0x00    | XPT Status 26   | 5:0  | OUT 26 [5:0] | Output 26 connection status                                      |
| 0x6F             | 0x00    | XPT Status 27   | 5:0  | OUT 27 [5:0] | Output 27 connection status                                      |
| 0x70             | 0x00    | XPT Status 28   | 5:0  | OUT 28 [5:0] | Output 28 connection status                                      |
| 0x71             | 0x00    | XPT Status 29   | 5:0  | OUT 29 [5:0] | Output 29 connection status                                      |
| 0x72             | 0x00    | XPT Status 30   | 5:0  | OUT 30 [5:0] | Output 30 connection status                                      |
| 0x73             | 0x00    | XPT Status 31   | 5:0  | OUT 31 [5:0] | Output 31 connection status                                      |
| 0x74             | 0x00    | XPT Status 32   | 5:0  | OUT 32 [5:0] | Output 32 connection status                                      |
| 0x75             | 0x00    | XPT Status 33   | 5:0  | OUT 33 [5:0] | Output 33 connection status                                      |
| 0x76             | 0x00    | XPT Status 34   | 5:0  | OUT 34 [5:0] | Output 34 connection status                                      |
| 0x77             | 0x00    | XPT Status 35   | 5:0  | OUT 35 [5:0] | Output 35 connection status                                      |
| 0x78             | 0x00    | XPT Status 36   | 5:0  | OUT 36 [5:0] | Output 36 connection status                                      |
| 0x79             | 0x00    | XPT Status 37   | 5:0  | OUT 37 [5:0] | Output 37 connection status                                      |
| 0x7A             | 0x00    | XPT Status 38   | 5:0  | OUT 38 [5:0] | Output 38 connection status                                      |
| 0x7B             | 0x00    | XPT Status 39   | 5:0  | OUT 39 [5:0] | Output 39 connection status                                      |
| 0x7D             | 0x00    | XPT Headroom    | 0    | XPT_HDROOM   | 0 = disabled, 1 = enabled (required when V <sub>CC</sub> > 2.7V) |
| 0x80: Output 0   | 0x40    | Tx Lane Control | 7    | Reserved     | 0 (Reserve bit)                                                  |
| 0x81: Output 1   | 0x40    | Tx Lane Control | 6:4  | OLEV [2:0]   | 000: 0 mA                                                        |
| 0x82: Output 2   | 0x40    | Tx Lane Control |      |              | 001: 4 mA                                                        |
| 0x83: Output 3   | 0x40    | Tx Lane Control |      |              | 010: 8 mA                                                        |
| 0x84: Output 4   | 0x40    | Tx Lane Control |      |              | 011: 12 mA                                                       |
| 0x85: Output 5   | 0x40    | Tx Lane Control |      |              | 100: 16 mA (default)                                             |
| 0x86: Output 6   | 0x40    | Tx Lane Control |      |              | 101: 20 mA                                                       |
| 0x87: Output 7   | 0x40    | Tx Lane Control |      |              | 110: 24 mA                                                       |
| 0x88: Output 8   | 0x40    | Tx Lane Control |      |              | 111: (Reserve bit)                                               |
| 0x89: Output 9   | 0x40    | Tx Lane Control |      |              |                                                                  |
| 0x8A: Output 10  | 0x40    | Tx Lane Control |      |              |                                                                  |
| 0x8B: Output 11  | 0x40    | Tx Lane Control | 3    | Overdrive    | 1: overdrive (increases OLEV and PE currents by 25%)             |
| 0x8C: Output 12  | 0x40    | Tx Lane Control |      |              | 0: no overdrive (default)                                        |
| 0x8D: Output 13  | 0x40    | Tx Lane Control |      |              |                                                                  |
| 0x8E: Output 14  | 0x40    | Tx Lane Control |      |              |                                                                  |
| 0x8F: Output 15  | 0x40    | Tx Lane Control | 2:0  | PE [2:0]     | 000: 0 mA (default)                                              |
| 0x90: Output 16  | 0x40    | Tx Lane Control |      |              | 001: 2 mA                                                        |
| 0x91: Output 17  | 0x40    | Tx Lane Control |      |              | 010: 3 mA                                                        |
| 0x92: Output 18  | 0x40    | Tx Lane Control |      |              | 011: 4 mA                                                        |
| 0x93: Output 19  | 0x40    | Tx Lane Control |      |              | 100: 5 mA                                                        |
| 0x94: Output 20  | 0x40    | Tx Lane Control |      |              | 101: 6 mA                                                        |
| 0x95: Output 21  | 0x40    | Tx Lane Control |      |              | 110: 7 mA                                                        |
| 0x96: Output 22  | 0x40    | Tx Lane Control |      |              | 111: 8 mA                                                        |
| 0x97: Output 23  | 0x40    | Tx Lane Control |      |              |                                                                  |
| 0x98: Output 24  | 0x40    | Tx Lane Control |      |              |                                                                  |

| Address: Channel   | Default | Register Name   | Bits | Bit Name    | Description                                                                  |
|--------------------|---------|-----------------|------|-------------|------------------------------------------------------------------------------|
| 0x99: Output 25    | 0x40    | Tx Lane Control |      |             |                                                                              |
| 0x9A: Output 26    | 0x40    | Tx Lane Control |      |             |                                                                              |
| 0x9B: Output 27    | 0x40    | Tx Lane Control |      |             |                                                                              |
| 0x9C: Output 28    | 0x40    | Tx Lane Control |      |             |                                                                              |
| 0x9D: Output 29    | 0x40    | Tx Lane Control |      |             |                                                                              |
| 0x9E: Output 30    | 0x40    | Tx Lane Control |      |             |                                                                              |
| 0x9F: Output 31    | 0x40    | Tx Lane Control |      |             |                                                                              |
| 0xA0: Output 32    | 0x40    | Tx Lane Control |      |             |                                                                              |
| 0xA1: Output 33    | 0x40    | Tx Lane Control |      |             |                                                                              |
| 0xA2: Output 34    | 0x40    | Tx Lane Control |      |             |                                                                              |
| 0xA3: Output 35    | 0x40    | Tx Lane Control |      |             |                                                                              |
| 0xA4: Output 36    | 0x40    | Tx Lane Control |      |             |                                                                              |
| 0xA5: Output 37    | 0x40    | Tx Lane Control |      |             |                                                                              |
| 0xA6: Output 38    | 0x40    | Tx Lane Control |      |             |                                                                              |
| 0xA7: Output 39    | 0x40    | Tx Lane Control |      |             |                                                                              |
| 0xA8: Tx Broadcast | 0x40    | Tx Lane Control |      |             |                                                                              |
| 0xA9               | 0x0     | Tx Sign Control | 7    | TXSIGN [7]  | Signal path polarity inversion Output 7<br>0 = noninverting<br>1 = inverting |
|                    |         |                 | 6    | TXSIGN [6]  | Signal path polarity inversion Output 6                                      |
|                    |         |                 | 5    | TXSIGN [5]  | Signal path polarity inversion Output 5                                      |
|                    |         |                 | 4    | TXSIGN [4]  | Signal path polarity inversion Output 4                                      |
|                    |         |                 | 3    | TXSIGN [3]  | Signal path polarity inversion Output 3                                      |
|                    |         |                 | 2    | TXSIGN [2]  | Signal path polarity inversion Output 2                                      |
|                    |         |                 | 1    | TXSIGN [1]  | Signal path polarity inversion Output 1                                      |
|                    |         |                 | 0    | TXSIGN [0]  | Signal path polarity inversion Output 0                                      |
| 0xAA               | 0x0     | Tx Sign Control | 7    | TXSIGN [15] | Signal path polarity inversion Output 15                                     |
|                    |         |                 | 6    | TXSIGN [14] | Signal path polarity inversion Output 14                                     |
|                    |         |                 | 5    | TXSIGN [13] | Signal path polarity inversion Output 13                                     |
|                    |         |                 | 4    | TXSIGN [12] | Signal path polarity inversion Output 12                                     |
|                    |         |                 | 3    | TXSIGN [11] | Signal path polarity inversion Output 11                                     |
|                    |         |                 | 2    | TXSIGN [10] | Signal path polarity inversion Output 10                                     |
|                    |         |                 | 1    | TXSIGN [9]  | Signal path polarity inversion Output 9                                      |
|                    |         |                 | 0    | TXSIGN [8]  | Signal path polarity inversion Output 8                                      |
| 0xAB               | 0x0     | Tx Sign Control | 7    | TXSIGN [23] | Signal path polarity inversion Output 23                                     |
|                    |         |                 | 6    | TXSIGN [22] | Signal path polarity inversion Output 22                                     |
|                    |         |                 | 5    | TXSIGN [21] | Signal path polarity inversion Output 21                                     |
|                    |         |                 | 4    | TXSIGN [20] | Signal path polarity inversion Output 20                                     |
|                    |         |                 | 3    | TXSIGN [19] | Signal path polarity inversion Output 19                                     |
|                    |         |                 | 2    | TXSIGN [18] | Signal path polarity inversion Output 18                                     |
|                    |         |                 | 1    | TXSIGN [17] | Signal path polarity inversion Output 17                                     |
|                    |         |                 | 0    | TXSIGN [16] | Signal path polarity inversion Output 16                                     |
| 0xAC               | 0x0     | Tx Sign Control | 7    | TXSIGN [31] | Signal path polarity inversion Output 31                                     |
|                    |         |                 | 6    | TXSIGN [30] | Signal path polarity inversion Output 30                                     |
|                    |         |                 | 5    | TXSIGN [29] | Signal path polarity inversion Output 29                                     |
|                    |         |                 | 4    | TXSIGN [28] | Signal path polarity inversion Output 28                                     |
|                    |         |                 | 3    | TXSIGN [27] | Signal path polarity inversion Output 27                                     |
|                    |         |                 | 2    | TXSIGN [26] | Signal path polarity inversion Output 26                                     |
|                    |         |                 | 1    | TXSIGN [25] | Signal path polarity inversion Output 25                                     |
|                    |         |                 | 0    | TXSIGN [24] | Signal path polarity inversion Output 24                                     |

| Address: Channel | Default | Register Name    | Bits | Bit Name    | Description                                                                                |
|------------------|---------|------------------|------|-------------|--------------------------------------------------------------------------------------------|
| 0xAD             | 0x0     | Tx Sign Control  | 7    | TXSIGN [39] | Signal path polarity inversion Output 39                                                   |
|                  |         |                  | 6    | TXSIGN [38] | Signal path polarity inversion Output 38                                                   |
|                  |         |                  | 5    | TXSIGN [37] | Signal path polarity inversion Output 37                                                   |
|                  |         |                  | 4    | TXSIGN [36] | Signal path polarity inversion Output 36                                                   |
|                  |         |                  | 3    | TXSIGN [35] | Signal path polarity inversion Output 35                                                   |
|                  |         |                  | 2    | TXSIGN [34] | Signal path polarity inversion Output 34                                                   |
|                  |         |                  | 1    | TXSIGN [33] | Signal path polarity inversion Output 33                                                   |
|                  |         |                  | 0    | TXSIGN [32] | Signal path polarity inversion Output 32                                                   |
| 0xB0             | 0x0     | Tx Drive Control | 7:6  | TXEN [3]    | Tx enable state Output 3<br>11 = enabled<br>10 = standby<br>01 = squelch<br>00 = disabled  |
|                  |         |                  | 5:4  | TXEN [2]    | Tx enable state Output 2                                                                   |
|                  |         |                  | 3:2  | TXEN [1]    | Tx enable state Output 1                                                                   |
|                  |         |                  | 1:0  | TXEN [0]    | Tx enable state Output 0                                                                   |
|                  |         |                  |      |             |                                                                                            |
| 0xB1             | 0x0     | Tx Drive Control | 7:6  | TXEN [7]    | Tx enable state Output 7<br>11 = enabled<br>10 = standby<br>01 = squelch<br>00 = disabled  |
|                  |         |                  | 5:4  | TXEN [6]    | Tx enable state Output 6                                                                   |
|                  |         |                  | 3:2  | TXEN [5]    | Tx enable state Output 5                                                                   |
|                  |         |                  | 1:0  | TXEN [4]    | Tx enable state Output 4                                                                   |
|                  |         |                  |      |             |                                                                                            |
| 0xB2             | 0x0     | Tx Drive Control | 7:6  | TXEN [11]   | Tx enable state Output 11<br>11 = enabled<br>10 = standby<br>01 = squelch<br>00 = disabled |
|                  |         |                  | 5:4  | TXEN [10]   | Tx enable state Output 10                                                                  |
|                  |         |                  | 3:2  | TXEN [9]    | Tx enable state Output 9                                                                   |
|                  |         |                  | 1:0  | TXEN [8]    | Tx enable state Output 8                                                                   |
|                  |         |                  |      |             |                                                                                            |
| 0xB3             | 0x0     | Tx Drive Control | 7:6  | TXEN [15]   | Tx enable state Output 15<br>11 = enabled<br>10 = standby<br>01 = squelch<br>00 = disabled |
|                  |         |                  | 5:4  | TXEN [14]   | Tx enable state Output 14                                                                  |
|                  |         |                  | 3:2  | TXEN [13]   | Tx enable state Output 13                                                                  |
|                  |         |                  | 1:0  | TXEN [12]   | Tx enable state Output 12                                                                  |
|                  |         |                  |      |             |                                                                                            |
| 0xB4             | 0x0     | Tx Drive Control | 7:6  | TXEN [19]   | Tx enable state Output 19<br>11 = enabled<br>10 = standby<br>01 = squelch<br>00 = disabled |
|                  |         |                  | 5:4  | TXEN [18]   | Tx enable state Output 18                                                                  |
|                  |         |                  | 3:2  | TXEN [17]   | Tx enable state Output 17                                                                  |
|                  |         |                  | 1:0  | TXEN [16]   | Tx enable state Output 16                                                                  |
|                  |         |                  |      |             |                                                                                            |

| Address: Channel | Default    | Register Name    | Bits | Bit Name    | Description                                                                                |
|------------------|------------|------------------|------|-------------|--------------------------------------------------------------------------------------------|
| 0xB5             | 0x0        | Tx Drive Control | 7:6  | TXEN [23]   | Tx enable state Output 23<br>11 = enabled<br>10 = standby<br>01 = squelch<br>00 = disabled |
|                  |            |                  | 5:4  | TXEN [22]   | Tx enable state Output 22                                                                  |
|                  |            |                  | 3:2  | TXEN [21]   | Tx enable state Output 21                                                                  |
|                  |            |                  | 1:0  | TXEN [20]   | Tx enable state Output 20                                                                  |
| 0xB6             | 0x0        | Tx Drive Control | 7:6  | TXEN [27]   | Tx enable state Output 27<br>11 = enabled<br>10 = standby<br>01 = squelch<br>00 = disabled |
|                  |            |                  | 5:4  | TXEN [26]   | Tx enable state Output 26                                                                  |
|                  |            |                  | 3:2  | TXEN [25]   | Tx enable state Output 25                                                                  |
|                  |            |                  | 1:0  | TXEN [24]   | Tx enable state Output 24                                                                  |
| 0xB7             | 0x0        | Tx Drive Control | 7:6  | TXEN [31]   | Tx enable state Output 31<br>11 = enabled<br>10 = standby<br>01 = squelch<br>00 = disabled |
|                  |            |                  | 5:4  | TXEN [30]   | Tx enable state Output 30                                                                  |
|                  |            |                  | 3:2  | TXEN [29]   | Tx enable state Output 29                                                                  |
|                  |            |                  | 1:0  | TXEN [28]   | Tx enable state Output 28                                                                  |
| 0xB8             | 0x0        | Tx Drive Control | 7:6  | TXEN [35]   | Tx enable state Output 35<br>11 = enabled<br>10 = standby<br>01 = squelch<br>00 = disabled |
|                  |            |                  | 5:4  | TXEN [34]   | Tx enable state Output 34                                                                  |
|                  |            |                  | 3:2  | TXEN [33]   | Tx enable state Output 33                                                                  |
|                  |            |                  | 1:0  | TXEN [32]   | Tx enable state Output 32                                                                  |
| 0xB9             | 0x0        | Tx Drive Control | 7:6  | TXEN [39]   | Tx enable state Output 39<br>11 = enabled<br>10 = standby<br>01 = squelch<br>00 = disabled |
|                  |            |                  | 5:4  | TXEN [38]   | Tx enable state Output 38                                                                  |
|                  |            |                  | 3:2  | TXEN [37]   | Tx enable state Output 37                                                                  |
|                  |            |                  | 1:0  | TXEN [36]   | Tx enable state Output 36                                                                  |
| 0xBA             | Write Only | Tx Drive Control | 7:6  | TXENBC [39] | Tx enable state broadcast<br>11 = enabled<br>10 = standby<br>01 = squelch<br>00 = disabled |
| 0xBB             | 0x0        | Tx Headroom      | 0    | TX_HDROOM   | 0 = disabled, 1 = enabled (required when $V_{CC} > 2.7\text{ V}$ )                         |

| Address: Channel | Default | Register Name          | Bits | Bit Name         | Description                                                                                       |
|------------------|---------|------------------------|------|------------------|---------------------------------------------------------------------------------------------------|
| 0xBC             | 0x0     | Tx Termination Control | 4    | TXA_TERM [19:16] | Output[19:16] (B side) termination control<br>0: terminations enabled<br>1: terminations disabled |
|                  |         |                        | 3    | TXA_TERM [15:12] | Output[15:12] (B side) termination control                                                        |
|                  |         |                        | 2    | TXA_TERM [11:8]  | Output[11:8] (B side) termination control                                                         |
|                  |         |                        | 1    | TXA_TERM [7:4]   | Output[7:4] (B side) termination control                                                          |
|                  |         |                        | 0    | TXA_TERM [3:0]   | Output[3:0] (B side) termination control                                                          |
| 0xBD             | 0x0     | Tx Termination Control | 4    | TXB_TERM [39:36] | Output[39:36] (B side) termination control<br>0: terminations enabled<br>1: terminations disabled |
|                  |         |                        | 3    | TXB_TERM [35:32] | Output[35:32] (B side) termination control                                                        |
|                  |         |                        | 2    | TXB_TERM [31:28] | Output[31:28] (B side) termination control                                                        |
|                  |         |                        | 1    | TXB_TERM [27:24] | Output[27:24] (B side) termination control                                                        |
|                  |         |                        | 0    | TXB_TERM [23:20] | Output[23:20] (B side) termination control                                                        |
| 0xC0             | 0x0     | Rx EQ Control          | 7:6  | RXEQIN [3]       | Equalizer boost control for Input 3<br>11 = 12 dB<br>10 = 6 dB<br>01 = 3 dB<br>00 = disabled      |
|                  |         |                        | 5:4  | RXEQIN [2]       | Equalizer boost control for Input 2                                                               |
|                  |         |                        | 3:2  | RXEQIN [1]       | Equalizer boost control for Input 1                                                               |
|                  |         |                        | 1:0  | RXEQIN [0]       | Equalizer boost control for Input 0                                                               |
| 0xC1             | 0x0     | Rx EQ Control          | 7:6  | RXEQIN [7]       | Equalizer boost control for Input 7<br>11 = 12 dB<br>10 = 6 dB<br>01 = 3 dB<br>00 = disabled      |
|                  |         |                        | 5:4  | RXEQIN [6]       | Equalizer boost control for Input 6                                                               |
|                  |         |                        | 3:2  | RXEQIN [5]       | Equalizer boost control for Input 5                                                               |
|                  |         |                        | 1:0  | RXEQIN [4]       | Equalizer boost control for Input 4                                                               |
| 0xC2             | 0x0     | Rx EQ Control          | 7:6  | RXEQIN [11]      | Equalizer boost control for Input 11<br>11 = 12 dB<br>10 = 6 dB<br>01 = 3 dB<br>00 = disabled     |
|                  |         |                        | 5:4  | RXEQIN [10]      | Equalizer boost control for Input 10                                                              |
|                  |         |                        | 3:2  | RXEQIN [9]       | Equalizer boost control for Input 9                                                               |
|                  |         |                        | 1:0  | RXEQIN [8]       | Equalizer boost control for Input 8                                                               |
| 0xC3             | 0x0     | Rx EQ Control          | 7:6  | RXEQIN [15]      | Equalizer boost control for Input 15<br>11 = 12 dB<br>10 = 6 dB<br>01 = 3 dB<br>00 = disabled     |
|                  |         |                        | 5:4  | RXEQIN [14]      | Equalizer boost control for Input 14                                                              |
|                  |         |                        | 3:2  | RXEQIN [13]      | Equalizer boost control for Input 13                                                              |
|                  |         |                        | 1:0  | RXEQIN [12]      | Equalizer boost control for Input 12                                                              |

| Address: Channel | Default | Register Name | Bits | Bit Name    | Description                                                                                     |
|------------------|---------|---------------|------|-------------|-------------------------------------------------------------------------------------------------|
| 0xC4             | 0x0     | Rx EQ Control | 7:6  | RXEQIN [19] | Equalizer boost control for Input 19<br>11 = 12 dB<br>10 = 6 dB<br>01 = 3 dB<br>00 = disabled   |
|                  |         |               | 5:4  | RXEQIN [18] | Equalizer boost control for Input 18                                                            |
|                  |         |               | 3:2  | RXEQIN [17] | Equalizer boost control for Input 17                                                            |
|                  |         |               | 1:0  | RXEQIN [16] | Equalizer boost control for Input 16                                                            |
| 0xC5             | 0x0     | Rx EQ Control | 7:6  | RXEQIN [23] | Equalizer boost control for Input 23<br>11 = 12 dB<br>10 = 6 dB<br>01 = 3 dB<br>00 = disabled   |
|                  |         |               | 5:4  | RXEQIN [22] | Equalizer boost control for Input 22                                                            |
|                  |         |               | 3:2  | RXEQIN [21] | Equalizer boost control for Input 21                                                            |
|                  |         |               | 1:0  | RXEQIN [20] | Equalizer boost control for Input 20                                                            |
| 0xC6             | 0x0     | Rx EQ Control | 7:6  | RXEQIN [27] | Equalizer boost control for Input 27<br>11 = 12 dB<br>10 = 6 dB<br>01 = 3 dB<br>00 = disabled   |
|                  |         |               | 5:4  | RXEQIN [26] | Equalizer boost control for Input 26                                                            |
|                  |         |               | 3:2  | RXEQIN [25] | Equalizer boost control for Input 25                                                            |
|                  |         |               | 1:0  | RXEQIN [24] | Equalizer boost control for Input 24                                                            |
| 0xC7             | 0x0     | Rx EQ Control | 7:6  | RXEQIN [31] | Equalizer boost control for Input 31<br>11 = 12 dB<br>10 = 6 dB<br>01 = 3 dB<br>00 = disabled   |
|                  |         |               | 5:4  | RXEQIN [30] | Equalizer boost control for Input 30                                                            |
|                  |         |               | 3:2  | RXEQIN [29] | Equalizer boost control for Input 29                                                            |
|                  |         |               | 1:0  | RXEQIN [28] | Equalizer boost control for Input 28                                                            |
| 0xC8             | 0x0     | Rx EQ Control | 7:6  | RXEQIN [35] | Equalizer boost control for Input 35<br>11 = 12 dB<br>10 = 6 dB<br>01 = 3 dB<br>00 = disabled   |
|                  |         |               | 5:4  | RXEQIN [34] | Equalizer boost control for Input 34                                                            |
|                  |         |               | 3:2  | RXEQIN [33] | Equalizer boost control for Input 33                                                            |
|                  |         |               | 1:0  | RXEQIN [32] | Equalizer boost control for Input 32                                                            |
| 0xC9             | 0x0     | Rx EQ Control | 7:6  | RXEQIN [39] | Equalizer boost control for Input 39<br>11 = 12 dB<br>10 = 6 dB<br>01 = 3 dB<br>00 = disabled   |
|                  |         |               | 5:4  | RXEQIN [38] | Equalizer boost control for Input 38                                                            |
|                  |         |               | 3:2  | RXEQIN [37] | Equalizer boost control for Input 37                                                            |
|                  |         |               | 1:0  | RXEQIN [36] | Equalizer boost control for Input 36                                                            |
| 0xCA             | 0x0     | Rx EQ Control | 1:0  | RXEQIN BC   | Equalizer boost control for all inputs<br>11 = 12 dB<br>10 = 6 dB<br>01 = 3 dB<br>00 = disabled |

| Address: Channel | Default | Register Name          | Bits | Bit Name         | Description                                                                                                    |
|------------------|---------|------------------------|------|------------------|----------------------------------------------------------------------------------------------------------------|
| 0xCB             | 0x0     | Rx Sign Control        | 7    | RXSIGN [7]       | Signal path polarity inversion Input 7                                                                         |
|                  |         |                        | 6    | RXSIGN [6]       | Signal path polarity inversion Input 6                                                                         |
|                  |         |                        | 5    | RXSIGN [5]       | Signal path polarity inversion Input 5                                                                         |
|                  |         |                        | 4    | RXSIGN [4]       | Signal path polarity inversion Input 4                                                                         |
|                  |         |                        | 3    | RXSIGN [3]       | Signal path polarity inversion Input 3                                                                         |
|                  |         |                        | 2    | RXSIGN [2]       | Signal path polarity inversion Input 2                                                                         |
|                  |         |                        | 1    | RXSIGN [1]       | Signal path polarity inversion Input 1                                                                         |
|                  |         |                        | 0    | RXSIGN [0]       | Signal path polarity inversion Input 0                                                                         |
| 0xCC             | 0x0     | Rx Sign Control        | 7    | RXSIGN [15]      | Signal path polarity inversion Input 15                                                                        |
|                  |         |                        | 6    | RXSIGN [14]      | Signal path polarity inversion Input 14                                                                        |
|                  |         |                        | 5    | RXSIGN [13]      | Signal path polarity inversion Input 13                                                                        |
|                  |         |                        | 4    | RXSIGN [12]      | Signal path polarity inversion Input 12                                                                        |
|                  |         |                        | 3    | RXSIGN [11]      | Signal path polarity inversion Input 11                                                                        |
|                  |         |                        | 2    | RXSIGN [10]      | Signal path polarity inversion Input 10                                                                        |
|                  |         |                        | 1    | RXSIGN [9]       | Signal path polarity inversion Input 9                                                                         |
|                  |         |                        | 0    | RXSIGN [8]       | Signal path polarity inversion Input 8                                                                         |
| 0xCD             | 0x0     | Rx Sign Control        | 7    | RXSIGN [23]      | Signal path polarity inversion Input 23                                                                        |
|                  |         |                        | 6    | RXSIGN [22]      | Signal path polarity inversion Input 22                                                                        |
|                  |         |                        | 5    | RXSIGN [21]      | Signal path polarity inversion Input 21                                                                        |
|                  |         |                        | 4    | RXSIGN [20]      | Signal path polarity inversion Input 20                                                                        |
|                  |         |                        | 3    | RXSIGN [19]      | Signal path polarity inversion Input 19                                                                        |
|                  |         |                        | 2    | RXSIGN [18]      | Signal path polarity inversion Input 18                                                                        |
|                  |         |                        | 1    | RXSIGN [17]      | Signal path polarity inversion Input 17                                                                        |
|                  |         |                        | 0    | RXSIGN [16]      | Signal path polarity inversion Input 16                                                                        |
| 0xCE             | 0x0     | Rx Sign Control        | 7    | RXSIGN [31]      | Signal path polarity inversion Input 31                                                                        |
|                  |         |                        | 6    | RXSIGN [30]      | Signal path polarity inversion Input 30                                                                        |
|                  |         |                        | 5    | RXSIGN [29]      | Signal path polarity inversion Input 29                                                                        |
|                  |         |                        | 4    | RXSIGN [28]      | Signal path polarity inversion Input 28                                                                        |
|                  |         |                        | 3    | RXSIGN [27]      | Signal path polarity inversion Input 27                                                                        |
|                  |         |                        | 2    | RXSIGN [26]      | Signal path polarity inversion Input 26                                                                        |
|                  |         |                        | 1    | RXSIGN [25]      | Signal path polarity inversion Input 25                                                                        |
|                  |         |                        | 0    | RXSIGN [24]      | Signal path polarity inversion Input 24                                                                        |
| 0xCF             | 0x0     | Rx Sign Control        | 7    | RXSIGN [39]      | Signal path polarity inversion Input 39                                                                        |
|                  |         |                        | 6    | RXSIGN [38]      | Signal path polarity inversion Input 38                                                                        |
|                  |         |                        | 5    | RXSIGN [37]      | Signal path polarity inversion Input 37                                                                        |
|                  |         |                        | 4    | RXSIGN [36]      | Signal path polarity inversion Input 36                                                                        |
|                  |         |                        | 3    | RXSIGN [35]      | Signal path polarity inversion Input 35                                                                        |
|                  |         |                        | 2    | RXSIGN [34]      | Signal path polarity inversion Input 34                                                                        |
|                  |         |                        | 1    | RXSIGN [33]      | Signal path polarity inversion Input 33                                                                        |
|                  |         |                        | 0    | RXSIGN [32]      | Signal path polarity inversion Input 32                                                                        |
| 0xD0             | 0x0     | Rx Termination Control | 4    | RXA_TERM [19:16] | Input[19:16] (A Side) termination control<br>0: termination control enabled<br>1: termination control disabled |
|                  |         |                        | 3    | RXA_TERM [15:12] | Input [15:12] (A side) termination control                                                                     |
|                  |         |                        | 2    | RXA_TERM [11:8]  | Input [11:8] (A side) termination control                                                                      |
|                  |         |                        | 1    | RXA_TERM [7:4]   | Input [7:4] (A side) termination control                                                                       |
|                  |         |                        | 0    | RXA_TERM [3:0]   | Input [3:0] (A side) termination control                                                                       |

| Address: Channel | Default | Register Name          | Bits | Bit Name         | Description                                                                                       |
|------------------|---------|------------------------|------|------------------|---------------------------------------------------------------------------------------------------|
| 0xD1             | 0x0     | Rx Termination Control | 4    | RXB_TERM [39:36] | Input [39:36] (B Side) termination control<br>0: terminations enabled<br>1: terminations disabled |
|                  |         |                        | 3    | RXB_TERM [35:32] | Input [35:32] (B Side) termination control                                                        |
|                  |         |                        | 2    | RXB_TERM [31:28] | Input [31:28] (B Side) termination control                                                        |
|                  |         |                        | 1    | RXB_TERM [27:24] | Input [27:24] (B Side) termination control                                                        |
|                  |         |                        | 0    | RXB_TERM [23:20] | Input [23:20] (B Side) termination control                                                        |

## APPLICATIONS INFORMATION

The ADN4605 is an asynchronous and protocol agnostic digital switch and, therefore, is applicable to a wide range of applications including network routing and digital video switching. The ADN4605 supports the data rates and signaling levels of HDMI®, DVI®, DisplayPort and SD-, HD-, and 3G-SDI digital video. The ADN4605 can be used to create matrix switches. An example block diagram of a  $40 \times 40$  matrix switch is shown in Figure 50. Since HDMI, DVI, and DisplayPort are quad lane

protocols, four ADN4605 s are used to create a full  $40 \times 40$  matrix switch. Smaller arrays, such as  $10 \times 10$  and  $20 \times 20$ , require one and two ADN4605 devices, respectively. Proper high speed PCB design techniques should be used to maintain the signal integrity of the high data rate signals. It is important to minimize the lane-to-lane skew and crosstalk in these applications.

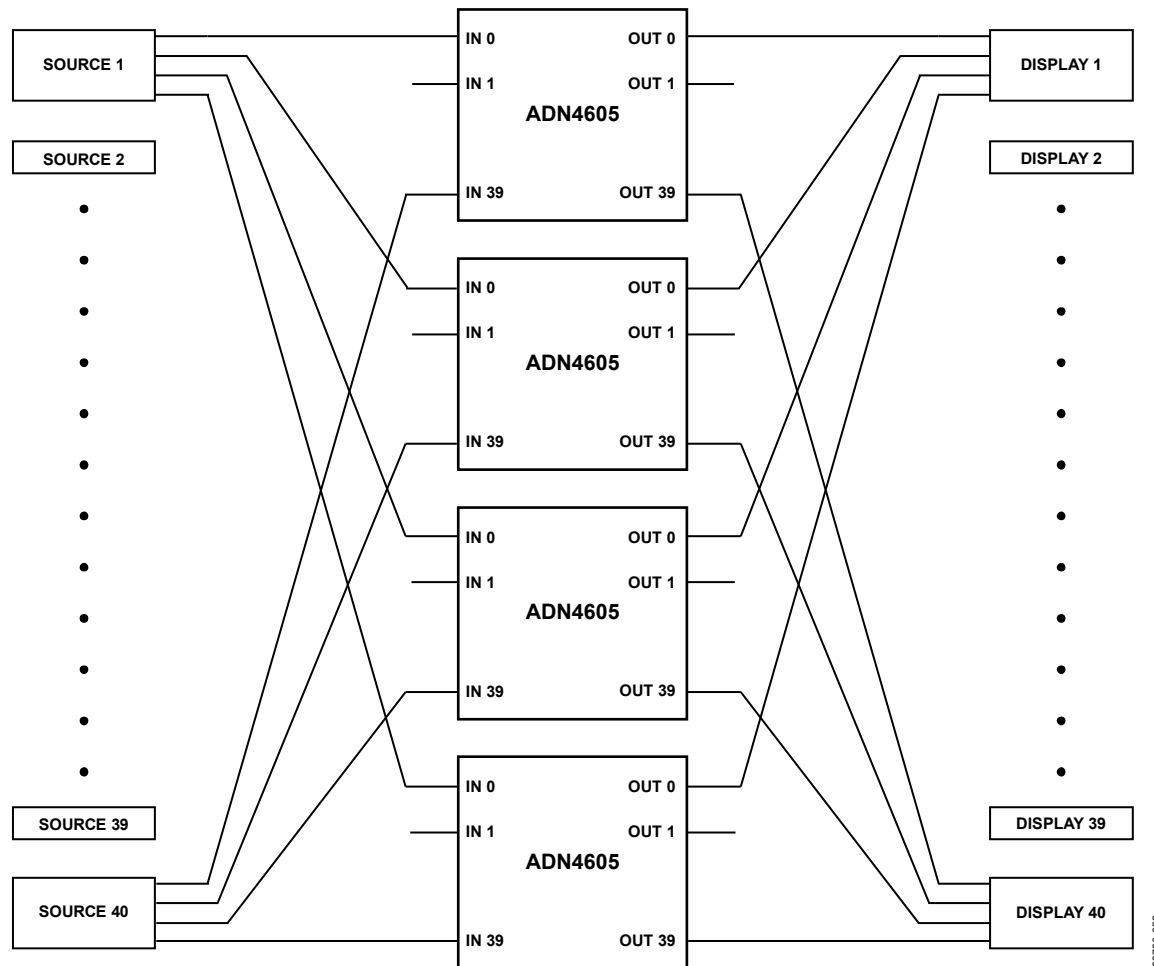


Figure 50. ADN4605 Digital Video (DVI, HDMI, Display Port) Matrix Switch Block Diagram

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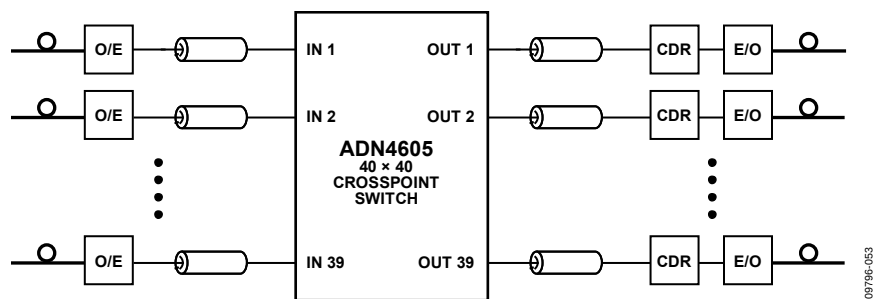


Figure 51. ADN4605 Networking Switch Application Block Diagram

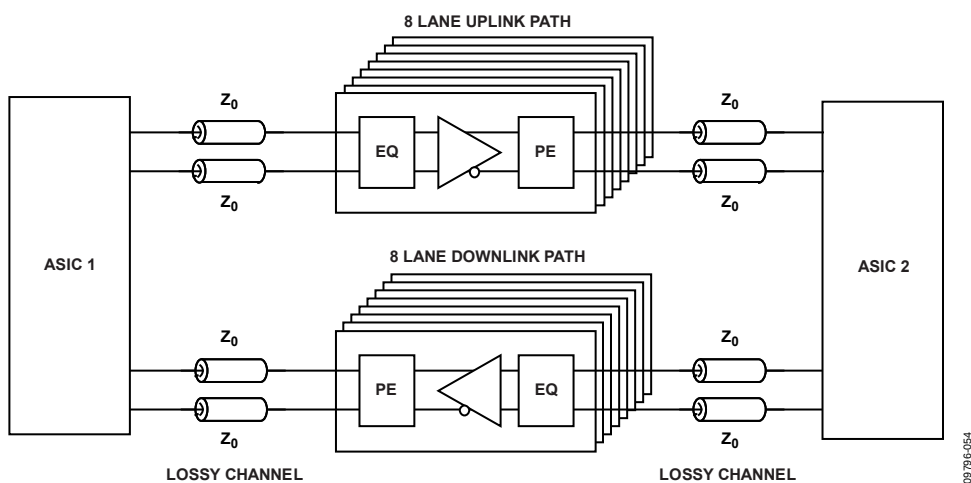


Figure 52. Multilane Signal Conditioning Application Diagram

## SUPPLY SEQUENCING

Ideally, all power supplies should be brought up to the appropriate levels simultaneously (power supply requirements are set by the supply limits in Table 1 and the absolute maximum ratings listed in Table 6).

If the power supplies to the ADN4605 are brought up separately, the supply power-up sequence is as follows:  $DV_{CC}$  powered first, followed by  $V_{CC}$ , and, last the termination supplies ( $V_{TTIA}$ ,  $V_{TTIB}$ ,  $V_{TTOA}$ , and  $V_{TTOB}$ ).

The power-down sequence is reversed with termination supplies being powered off first. The termination supplies contain ESD protection diodes to the  $V_{CC}$  power domain. To avoid a sustained high current condition in these devices, the  $V_{TTIx}$  and  $V_{TTOx}$  supplies should be powered on after  $V_{CC}$  and should be powered off before  $V_{CC}$ .

If the system power supplies have a high impedance in the powered off state, then supply sequencing is not required provided the following limits are observed:

- Peak current from  $V_{TTIx}$  or  $V_{TTOx}$  to  $V_{CC} < 200$  mA
- Sustained current from  $V_{TTIx}$  or  $V_{TTOx}$  to  $V_{CC} < 100$  mA

## POWER DISSIPATION

The power dissipation of the ADN4605 depends on the supply voltages, I/O coupling type, and device configuration. The input termination resistors dissipate power depending on the differential input swing and common-mode voltage. When ac-coupled, the common-mode voltage is equal to the termination supply voltage ( $V_{TTIx}$  or  $V_{TTOx}$ ). While the current drawn from the input termination supply is effectively zero, there is still power and heat dissipated in the termination resistors as a result of the differential signal swing. The core supply current and output termination current are strongly dependent on device configuration, such as the number of channels enabled, output level setting, and output preemphasis setting.

In high ambient temperature operating conditions, it is important to avoid exceeding the maximum junction temperature of the device. Limiting the total power dissipation can be achieved by the following:

- Reducing the output swing
- Reducing the preemphasis level
- Decreasing the supply voltages within the allowable ranges defined in Table 1
- Disabling unused channels

Alternatively, the thermal resistance can be reduced by

- Adding an external heat sink
- Increasing the airflow

Refer to the PCB Layout Guidelines section for recommendations for proper thermal stencil layout and fabrication.

## OUTPUT COMPLIANCE

In low voltage applications, users must pay careful attention to both the differential and common-mode signal levels. The choice of output voltage swing, preemphasis setting, supply voltages ( $V_{CC}$  and  $V_{TTOx}$ ), and output coupling (ac or dc) affect peak and settled single-ended voltage swings and the common-mode shift measured across the output termination resistors. These choices also affect output current and, consequently, power consumption.

Table 21 shows the change in output common mode ( $\Delta V_{OCM} = V_{CC} - V_{OCM}$ ) with output level and preemphasis setting. Single-ended output levels are calculated for  $V_{TTOx}$  supplies of 3.3 V and 2.5 V to illustrate practical challenges of reducing the supply voltage. The minimum  $V_L$  (min  $V_L$ ) cannot be below the absolute minimum level specified in Table 1.

Since the absolute minimum output voltage specified in Table 1 is relative to  $V_{CC}$ , decreasing  $V_{CC}$  is required to maintain the output levels within the specified limits when lower output termination voltages are required.  $V_{TTOx}$  voltages as low as 1.8 V are allowable for output swings less than or equal to 400 mV (single-ended).

Figure 53 illustrates an application where the ADN4605 is used as a dc-coupled level translator to interface a 3.3 V CML driver to an ASIC with 1.8 V I/Os. The diode in series with  $V_{CC}$  reduces the voltage at  $V_{CC}$  for improved output compliance.

## TX/XPT HEADROOM

The Tx Headroom and XPT Headroom registers are provided to improve the output compliance range of the ADN4605 when the core supply voltage ( $V_{CC}$ ) is greater than 2.7 V. Enabling the XPT Headroom and Tx Headroom registers allows the transmitter an extra 300 mV of output compliance. The headroom circuitry should not be enabled when the core supply voltage ( $V_{CC}$ ) is less than or equal to 2.7 V.

When set to 1, the XPT Headroom (Address 0x7D) and Tx Headroom (Address 0xBB) registers are enabled for all transmitter outputs. A value of 0 disables the headroom generating circuitry. Note that both registers (XPT Headroom and Tx Headroom) must be set for the headroom circuitry to function properly.

**Example:  $V_{CC} = 3.3\text{ V}$ ,  $V_{TTOx} = 2.5\text{ V}$** 

In a typical application, the user can select a default output level of 200 mV single-ended (400 mVp-p differential) and may want the option to choose preemphasis settings of 0 dB and 9.5 dB.

With preemphasis disabled, a dc-coupled transmitter causes a 100 mV common-mode shift across the termination resistors, whereas an ac-coupled transmitter causes twice the common-mode shift. When dc-coupled, the single-ended output voltage swings between 2.5 V and 2.3 V and between 2.4 V and 2.2 V when ac-coupled. In both cases, these levels are greater than the minimum  $V_L$  limit of 1.9 V ( $V_L = V_{CC} - 1.4\text{ V}$ ).

With a PE setting of 9.5 dB, the ac-coupled transmitter has single-ended swings from 2.2 V and 1.6 V, whereas the dc-coupled transmitter outputs swing between 2.5 V and 1.9 V. The minimum single-ended output voltage ( $V_{L-PE}$ ) of the ac-coupled transmitter case exceeds the minimum  $V_L$  limit of 1.9 V by 300 mV, violating the device specification.

Enabling the TX\_HDROOM and XPT\_HDROOM bit lowers the minimum  $V_L$  limit by approximately 300 mV to 1.6 V. This transmitter configuration now complies with the output voltage range specification.

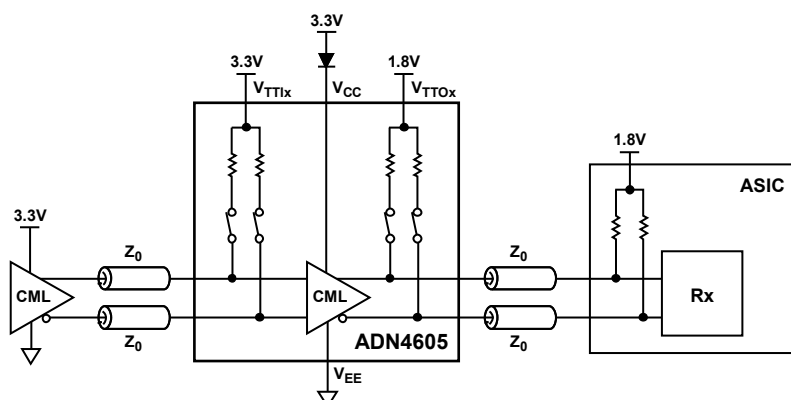


Figure 53. DC-Coupled Level Translator Application Circuit

Table 21. Output Voltage Range and Output Common-Mode Shift vs. Output Level and PE Setting

| Single-Ended Output Levels and PE Boost |                    |            |         | Tx Lane Control Register Settings |          | Output Current   | AC-Coupled Outputs                |                  |                                   |                  | DC-Coupled Outputs                |                         |                                   |                  |                  |                  |
|-----------------------------------------|--------------------|------------|---------|-----------------------------------|----------|------------------|-----------------------------------|------------------|-----------------------------------|------------------|-----------------------------------|-------------------------|-----------------------------------|------------------|------------------|------------------|
|                                         |                    |            |         |                                   |          |                  | $V_{CC} = V_{TTO} = 3.3\text{ V}$ |                  | $V_{CC} = V_{TTO} = 2.5\text{ V}$ |                  | $V_{CC} = V_{TTO} = 3.3\text{ V}$ |                         | $V_{CC} = V_{TTO} = 2.5\text{ V}$ |                  |                  |                  |
| $V_{SW-DC}^1$ (mV)                      | $V_{SW-PE}^1$ (mV) | PE Boost % | PE (dB) | OLEV [2:0]                        | PE [2:0] | $I_{TTO}^1$ (mA) | $\Delta V_{OCM}^1$ (mV)           | $V_{H-PE}^1$ (V) | $V_{L-PE}^1$ (V)                  | $V_{H-PE}^1$ (V) | $V_{L-PE}^1$ (V)                  | $\Delta V_{OCM}^1$ (mV) | $V_{H-PE}^1$ (V)                  | $V_{L-PE}^1$ (V) | $V_{H-PE}^1$ (V) | $V_{L-PE}^1$ (V) |
| 100                                     | 100                | 0.00       | 0.00    | 0x01                              | 0x00     | 4                | 100                               | 3.25             | 3.15                              | 2.45             | 2.35                              | 50                      | 3.3                               | 3.2              | 2.5              | 2.4              |
| 100                                     | 300                | 200.00     | 9.54    | 0x02                              | 0x03     | 12               | 300                               | 3.15             | 2.85                              | 2.35             | 2.05                              | 150                     | 3.3                               | 3.0              | 2.5              | 2.2              |
| 100                                     | 500                | 400.00     | 13.98   | 0x03                              | 0x07     | 20               | 500                               | 3.05             | 2.55                              | 2.25             | 1.75                              | 250                     | 3.3                               | 2.8              | 2.5              | 2.0              |
| 150                                     | 250                | 66.67      | 4.44    | 0x02                              | 0x01     | 10               | 250                               | 3.175            | 2.925                             | 2.375            | 2.125                             | 125                     | 3.3                               | 3.15             | 2.5              | 2.25             |
| 150                                     | 450                | 200.00     | 9.54    | 0x03                              | 0x05     | 18               | 450                               | 3.075            | 2.625                             | 2.275            | 1.825                             | 225                     | 3.3                               | 2.85             | 2.5              | 2.05             |
| 200                                     | 200                | 0.00       | 0.00    | 0x02                              | 0x00     | 8                | 200                               | 3.2              | 3.0                               | 2.40             | 2.20                              | 100                     | 3.3                               | 3.1              | 2.5              | 2.3              |
| 200                                     | 400                | 100.00     | 6.02    | 0x03                              | 0x03     | 16               | 400                               | 3.1              | 2.7                               | 2.30             | 1.90                              | 200                     | 3.3                               | 2.9              | 2.5              | 2.1              |
| 200                                     | 600                | 200.00     | 9.54    | 0x04                              | 0x07     | 24               | 600                               | 3                | 2.4                               | 2.20             | 1.60                              | 300                     | 3.3                               | 2.7              | 2.5              | 1.9              |
| 250                                     | 350                | 40.00      | 2.92    | 0x03                              | 0x01     | 14               | 350                               | 3.125            | 2.775                             | 2.325            | 1.975                             | 175                     | 3.3                               | 2.95             | 2.5              | 2.15             |
| 250                                     | 550                | 200.00     | 6.85    | 0x04                              | 0x05     | 22               | 550                               | 3.025            | 2.475                             | 2.225            | 1.675                             | 275                     | 3.3                               | 2.75             | 2.5              | 1.95             |
| 300                                     | 300                | 0.00       | 0.00    | 0x03                              | 0x00     | 12               | 300                               | 3.15             | 2.85                              | 2.35             | 2.05                              | 150                     | 3.3                               | 3.0              | 2.5              | 2.2              |
| 300                                     | 500                | 66.67      | 4.44    | 0x04                              | 0x03     | 20               | 500                               | 3.05             | 2.55                              | 2.25             | 1.75                              | 250                     | 3.3                               | 2.8              | 2.5              | 2.0              |
| 300                                     | 700                | 133.33     | 7.36    | 0x05                              | 0x07     | 28               | 700                               | 2.95             | 2.25                              | 2.15             | 1.45                              | 350                     | 3.3                               | 2.6              | 2.5              | 1.8              |
| 350                                     | 450                | 28.57      | 2.18    | 0x04                              | 0x01     | 18               | 450                               | 3.075            | 2.625                             | 2.275            | 1.825                             | 225                     | 3.3                               | 2.85             | 2.5              | 2.05             |
| 350                                     | 650                | 85.71      | 5.38    | 0x05                              | 0x05     | 26               | 650                               | 2.975            | 2.325                             | 2.175            | 1.525                             | 325                     | 3.3                               | 2.65             | 2.5              | 1.85             |
| 400                                     | 400                | 0.00       | 0.00    | 0x04                              | 0x00     | 16               | 400                               | 3.1              | 2.7                               | 2.3              | 1.9                               | 200                     | 3.3                               | 2.9              | 2.5              | 2.1              |
| 400                                     | 600                | 50.00      | 3.52    | 0x05                              | 0x03     | 24               | 600                               | 3.0              | 2.4                               | 2.2              | 1.6                               | 300                     | 3.3                               | 2.7              | 2.5              | 1.9              |
| 400                                     | 800                | 100.00     | 6.02    | 0x06                              | 0x07     | 32               | 800                               | 2.9              | 2.1                               | 2.1              | 1.3                               | 400                     | 3.3                               | 2.5              | 2.5              | 1.7              |
| 450                                     | 550                | 22.22      | 1.74    | 0x05                              | 0x01     | 22               | 550                               | 3.025            | 2.475                             | 2.225            | 1.675                             | 275                     | 3.3                               | 2.75             | 2.5              | 1.95             |
| 450                                     | 750                | 66.67      | 4.44    | 0x06                              | 0x05     | 30               | 750                               | 2.925            | 2.175                             | 2.125            | 1.375                             | 375                     | 3.3                               | 2.55             | 2.5              | 1.75             |
| 500                                     | 500                | 0.00       | 0.00    | 0x05                              | 0x00     | 20               | 500                               | 3.05             | 2.55                              | 2.25             | 1.75                              | 250                     | 3.3                               | 2.8              | 2.5              | 2.0              |
| 500                                     | 700                | 40.00      | 2.92    | 0x06                              | 0x03     | 28               | 700                               | 2.95             | 2.25                              | 2.15             | 1.45                              | 350                     | 3.3                               | 2.6              | 2.5              | 1.8              |
| 550                                     | 650                | 18.18      | 1.45    | 0x06                              | 0x01     | 26               | 650                               | 2.975            | 2.325                             | 2.175            | 1.525                             | 325                     | 3.3                               | 2.65             | 2.5              | 1.85             |
| 600                                     | 600                | 0.00       | 0.00    | 0x06                              | 0x00     | 24               | 600                               | 3.0              | 2.4                               | 2.2              | 1.6                               | 300                     | 3.3                               | 2.7              | 2.5              | 1.9              |

<sup>1</sup> Symbol definitions are shown in Table 16.

PCB LAYOUT GUIDELINES

The high speed differential inputs and outputs should be routed with 100 Ω controlled impedance differential transmission lines. The transmission lines, either microstrip or stripline, should be referenced to a solid low impedance reference plane. An example of a PCB cross-section is shown in Figure 54. The trace width (W), differential spacing (S), height above reference plane (H), and dielectric constant of the PCB material determine the characteristic impedance. Adjacent channels should be kept apart by a distance greater than 3 W to minimize crosstalk.

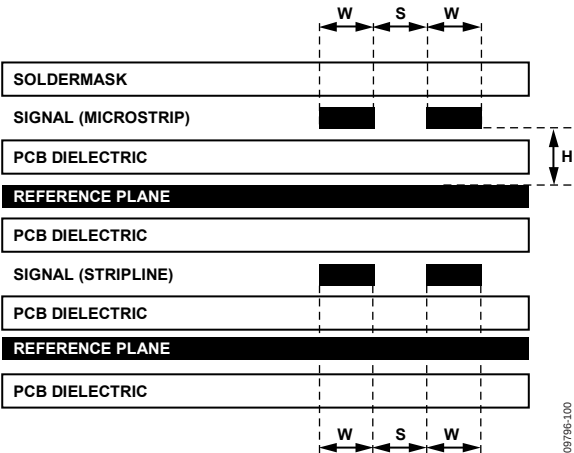


Figure 54. Example of a PCB Cross Section

## OUTLINE DIMENSIONS

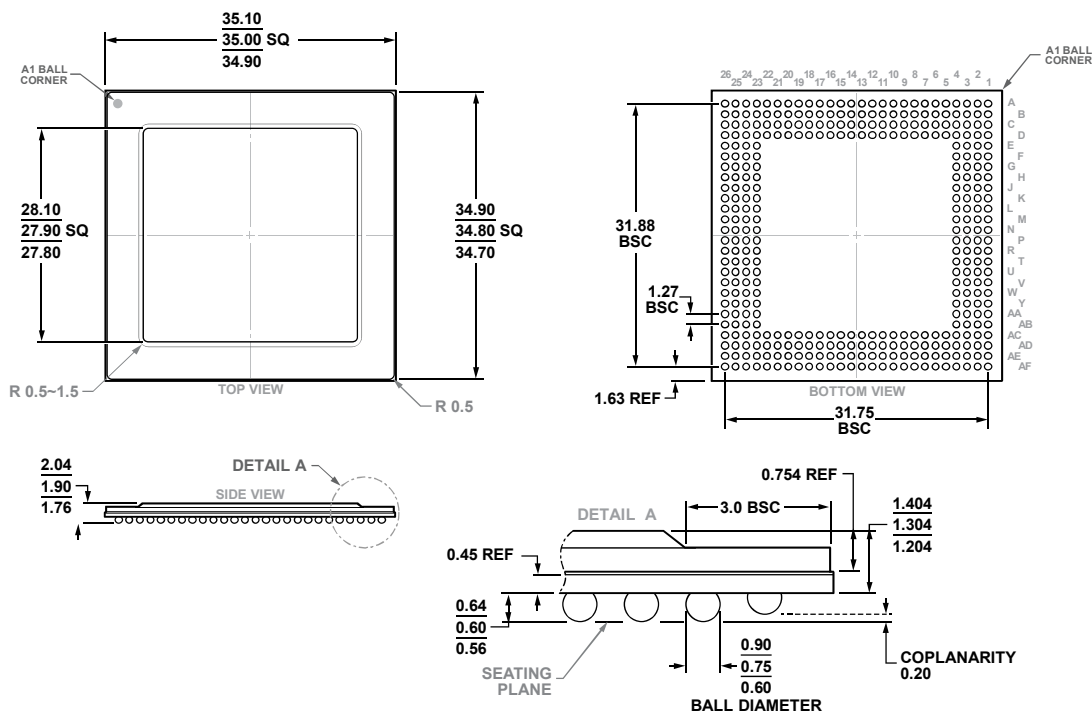


Figure 55. 352-Ball Ball Grid Array, Thermally Enhanced [BGA\_ED]  
(BP-352-2)  
Dimensions shown in millimeters

## ORDERING GUIDE

| Model <sup>1</sup> | Temperature Range | Package Description                                   | Package Option |
|--------------------|-------------------|-------------------------------------------------------|----------------|
| ADN4605ABPZ        | –40°C to +85°C    | 352-Ball Ball Grid Array, Thermally Enhanced [BGA_ED] | BP-352-2       |
| ADN4605-EVALZ      |                   | Evaluation Board                                      |                |

<sup>1</sup>Z = RoHS Compliant Part.

## NOTES

I<sup>2</sup>C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

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